



UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 1614.1074

First Named Inventor or Application Identifier:

Hideo MIYAKE et al.

Express Mail Label No.

JC639 U.S. PTO 09/654527 09/01/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231**

1. Fee Transmittal Form
2. Specification, Claims & Abstract [Total Pages: 58]
3. Drawing(s) (35 USC 113) [Total Sheets: 39]
4. Oath or Declaration [Total Pages: 4]
 a. Newly executed (original or copy)
 b. Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional with Box 17 completed)
 i. **DELETION OF INVENTOR(S)**
 Signed statement attached deleting inventor(s) named in the prior application,
 see 37 CFR 1.63(d)(2) and 1.33(b).
5. Incorporation by Reference (usable if Box 4b is checked)
 The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. Microfiche Computer Program (*Appendix*)
7. Nucleotide and/or Amino Acid Sequence Submission (*if applicable, all necessary*)
 a. Computer Readable Copy
 b. Paper Copy (identical to computer copy)
 c. Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. Assignment Papers (cover sheet & document(s))
9. 37 CFR 3.73(b) Statement (*when there is an assignee*) Power of Attorney
10. English Translation Document (*if applicable*)
11. Information Disclosure Statement (IDS)/PTO-1449 Copies of IDS Citations
12. Preliminary Amendment
13. Return Receipt Postcard (MPEP 503) (*Should be specifically itemized*)
14. Small Entity Statement(s) Statement filed in prior application, status still proper and desired.
15. Certified Copy of Priority Document(s) (*if foreign priority is claimed*)
16. Other:

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

Continuation Divisional Continuation-in-part (CIP) of prior application No: /

18. CORRESPONDENCE ADDRESS



21171

PATENT TRADEMARK OFFICE

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT WE, Hideo Miyake, a citizen of Japan residing at Kawasaki, Japan, Atsuhiro Suga, a citizen of Japan residing at Kawasaki, Japan, Yasuki Nakamura, a citizen of Japan residing at Kawasaki, Japan and Yoshimasa Takebe, a citizen of Japan residing at Kawasaki, Japan have invented certain new and useful improvements in

PARALLEL PROCESSOR

of which the following is a specification : -

TITLE OF THE INVENTION

BACKGROUND OF THE INVENTION

5 1. Field of the Invention

The present invention generally relates to processors, and, more particularly, to a parallel processor that executes a plurality of basic instructions in parallel.

2. Description of the Related Art

Generally, in a conventional computer system, a plurality of basic instructions are executed in parallel by pipeline processing, thereby improving its performance. Conventionally, a

15 plurality of basic instructions constitute a fixed-length instruction word, and a very-long instruction word (VLIW) technique is employed as a method for organizing a plurality of basic instructions.

20 contained in one instruction word in parallel. Also, a super scalar technique may be employed. In accordance with the super scalar technique, basic instructions are executed in parallel depending on the number of basic instructions contained in each instruction word.

25 FIG. 1 shows the structure of a conventional parallel processor 10. This parallel processor 10 comprises an instruction fetch unit 1 connected to a memory 7, an instruction issue unit 3

30 instruction execution units EU0 to EU_n each connected to the instruction issue unit 3, and a register unit 5 connected to each of the instruction execution units EU0 to EU_n.

35 The instruction fetch unit 1 fetches an instruction word from the memory 7, and supplies the instruction word to the instruction issue unit 3. The instruction issue unit 3 issues the basic

instructions contained in the supplied instruction word to the instruction execution units EU0 to EU_n. If the instruction execution units EU0 to EU_n are still executing previous basic instructions at this 5 point, the instruction issue unit 3 waits for the end of the execution. When the execution ends, the instruction issue unit 3 supplies the basic instructions to the instruction execution units EU0 to EU_n.

10 The instruction execution units EU0 to EU_n execute the basic instructions, and notify the instruction issue unit 3 of the end of the execution. The register unit 5 supplies data to the instruction execution units EU0 to EU_n, if necessary, and holds 15 the execution results of the instruction execution units EU0 to EU_n. The externally connected memory 7 stores a instruction word string to be executed in the parallel processor 10. The memory 7 also stores necessary data for the execution units EU0 to EU_n to 20 execute instructions, and data as the execution results.

FIG. 2 shows the formats of instruction words to be supplied to a parallel processor having four instruction execution units EU0 to EU3. As 25 shown in FIG. 2, each instruction word is made up of a basic instruction EI and a do-nothing instruction NOP. If the number of basic instructions contained in one instruction word to be executed in parallel is smaller than the number of the instruction execution units EU0 to EU3, the proportion of do-nothing 30 instructions is large.

In the conventional parallel processing method of executing a plurality of basic instructions by the VLIW technique, each instruction 35 word has a fixed length. Therefore, if the number of basic instructions to be executed in parallel is smaller than a predetermined number, do-nothing

instructions are added to comply with the predetermined length. Because of that, in a program having a small number of basic instructions in total, the proportion of do-nothing instructions is large, and the amount of instruction code increases accordingly, resulting in problems such as poor usage efficiency of memory, a decrease of the hit ratio of cache memory, and an increase of the load on the instruction fetch mechanism.

With the super scalar technique, there is also a problem that a large-scale circuit is needed to increase the number of instructions to be executed in parallel.

15 SUMMARY OF THE INVENTION

A general object of the present invention is to provide parallel processors in which the above disadvantages are eliminated.

20 A more specific object of the present invention is to provide a parallel processor that is capable of performing highly efficient parallel processing.

The above objects of the present invention are achieved by a parallel processor that performs parallel processing of one or more basic instructions contained in each of instruction words delimited by instruction delimiting information, the parallel processor comprising:

30 a plurality of instruction execution units that perform processes corresponding to the supplied basic instructions in parallel;

an instruction fetch unit that fetches the instruction words one by one in accordance with the instruction delimiting information; and

35 an instruction issue unit that selectively issues each of the basic instructions supplied from the instruction fetch unit to one of the instruction

execution units to execute the basic instruction.

With the parallel processor having the above structure, the instruction fetch unit makes each instruction word length variable, so that the 5 instruction words can be fetched one by one in accordance with the instruction delimiting information. Also, the instruction execution units can efficiently execute the instruction words, because each of the basic instructions is 10 selectively issued to a corresponding one of the instruction execution units.

The above and other objects and features of the present invention will become more apparent from the following description taken in conjunction 15 with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows the structure of a conventional parallel processor;

20 FIG. 2 shows the formats of instruction words to be supplied to a conventional parallel processor having four instruction execution units;

FIG. 3 shows the structure of a first example of a parallel processor in accordance with a 25 first embodiment of the present invention;

FIG. 4 shows the structures of an instruction fetch unit and an instruction issue unit of the parallel processor shown in FIG. 3;

30 FIG. 5 shows the formats of instruction words to be supplied to the parallel processor of the first embodiment of the present invention;

FIG. 6 shows the structure of a second example of the parallel processor in accordance with the first embodiment of the present invention;

35 FIG. 7 shows the structure of a first example of a parallel processor in accordance with a second embodiment of the present invention;

FIG. 8 shows the structures of an instruction fetch unit and an instruction issue unit of the parallel processor shown in FIG. 7;

FIG. 9 illustrates basic instruction rearrangement in the parallel processor of the second embodiment of the present invention;

FIG. 10 is a circuit diagram of a conversion unit in the parallel processor shown in FIG. 7;

10 FIG. 11 is a circuit diagram of the
conversion unit in a case where the maximum basic
instruction word length is 4;

FIG. 12 shows the structure of a second example of the parallel processor in accordance with the second embodiment of the present invention;

FIG. 13 shows the structures of an instruction fetch unit and an instruction issue unit of the parallel processor shown in FIG. 12;

FIG. 14 shows the structure of a third example of the parallel processor in accordance with the second embodiment of the present invention;

FIG. 15 shows the structures of an instruction fetch unit and an instruction issue unit of the parallel processor shown in FIG. 14;

25 FIG. 16 shows the structure of a fourth example of the parallel processor in accordance with the second embodiment of the present invention;

FIG. 17 shows the structures of an instruction fetch unit and an instruction issue unit of the parallel processor shown in FIG. 16;

FIG. 18 shows the structure of a fifth example of the parallel processor in accordance with the second embodiment of the present invention;

35 FIG. 19 shows the structures of an instruction fetch unit and an instruction issue unit of the parallel processor shown in FIG. 18;

FIG. 20 shows the structure of a sixth

example of the parallel processor in accordance with the second embodiment of the present invention;

5 FIG. 21 shows the structures of an instruction fetch unit and an instruction issue unit of the parallel processor shown in FIG. 20;

FIG. 22 shows the structure of a first example of a parallel processor in accordance with a third embodiment of the present invention;

10 FIG. 23 shows the structure of a second example of the parallel processor in accordance with the third embodiment of the present invention;

FIG. 24 shows the structure of a third example of the parallel processor in accordance with the third embodiment of the present invention;

15 FIG. 25 shows the structure of a fourth example of the parallel processor in accordance with the third embodiment of the present invention;

20 FIG. 26 shows the structure of a fifth example of the parallel processor in accordance with the third embodiment of the present invention;

FIG. 27 shows the structure of a sixth example of the parallel processor in accordance with the third embodiment of the present invention;

25 FIG. 28 shows the structure of a first example of a parallel processor in accordance with a fourth embodiment of the present invention;

FIG. 29 shows the structure of a second example of the parallel processor in accordance with the fourth embodiment of the present invention;

30 FIG. 30 shows the structure of a third example of the parallel processor in accordance with the fourth embodiment of the present invention;

35 FIG. 31 shows the structure of a fourth example of the parallel processor in accordance with the fourth embodiment of the present invention;

FIG. 32 shows the structure of a fifth example of the parallel processor in accordance with

the fourth embodiment of the present invention;

FIG. 33 shows the structure of a sixth example of the parallel processor in accordance with the fourth embodiment of the present invention;

5 FIG. 34 shows the structure of a first example of a parallel processor in accordance with a fifth embodiment of the present invention;

10 FIG. 35 shows the structure of a second example of the parallel processor in accordance with the fifth embodiment of the present invention;

FIG. 36 shows the structure of a third example of the parallel processor in accordance with the fifth embodiment of the present invention;

15 FIG. 37 shows the structure of a fourth example of the parallel processor in accordance with the fifth embodiment of the present invention;

FIG. 38 shows the structure of a fifth example of the parallel processor in accordance with the fifth embodiment of the present invention; and

20 FIG. 39 shows the structure of a sixth example of the parallel processor in accordance with the fifth embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

25 The following is a description of embodiments of the present invention, with reference to the accompanying drawings.

[Embodiment 1]

30 FIGS. 3 and 6 show parallel processors 20 and 21 in accordance with a first embodiment of the present invention. The parallel processor 20 comprises an instruction fetch unit 46 connected to a memory 12, an instruction issue unit 72 connected 35 to the instruction fetch unit 46, two instruction execution units EU0 and EU1 having the same structure and connected to the instruction issue

unit 72, and a register unit 98 connected to each of the instruction execution units EU0 and EU1. Likewise, the parallel processor 21 comprises an instruction fetch unit 47 connected to a memory 12, 5 an instruction issue unit 73 connected to the instruction fetch unit 47, two instruction execution units EU0 and EU1 having the same structure and connected to the instruction issue unit 73, and a register unit 98 connected to each of the 10 instruction execution units EU0 and EU1.

It should be noted that, in the following description, the maximum basic instruction length of one instruction word is 2. However, the parallel processor in accordance with the first embodiment 15 should operate in the same manner in a case where the maximum basic instruction length in one instruction word is 3 or greater.

(Example 1)

FIG. 4 shows the structure of the 20 instruction fetch unit 46 and the instruction issue unit 72. The instruction fetch unit 46 comprises a fetch program counter (FPC) 300, adders 324 and 325, an instruction buffer 308, a cutting unit 316, and an execution program counter (EPC) 339.

25 The FPC 300 is connected to the memory 12 and the instruction execution units EU0 and EU1. The adder 324 is connected to the FPC 300. The instruction buffer 308 is connected to the memory 12, and the cutting unit 316 is connected to the 30 instruction buffer 308. The adder 325 is connected to the cutting unit 316, and the EPC 339 is connected to the adder 325 and the register unit 98. The FPC 300 receives a fetch address contained in an instruction word from the memory 12, and the 35 instruction buffer 308 receives fetch data contained in the instruction word from the memory 12. The FPC 300 further receives a branch destination address

corresponding to a branch instruction from the instruction execution units EU0 and EU1.

On the other hand, the instruction issue unit 72 comprises an instruction register 347, 5 selectors 355 and 356, a control unit 370, and an AND gate 378. Here, the instruction register 347 is connected to the cutting unit 316. The selectors 355 and 356 are both connected to the instruction register 347. The selector 355 is connected to the 10 instruction execution unit EU0, while the selector 356 is connected to the instruction execution unit EU1. The control unit 370 is connected to the AND gate 378 and the selectors 355 and 356. The AND gate is connected to the instruction execution 15 units EU0 and EU1. In this structure, the instruction execution units EU0 and EU1 transmit execution complete signals EUc0 and EUc1, respectively, to the AND gate 378.

FIG. 5 shows the formats of instruction words to be supplied to the parallel processors of the first embodiment. Each instruction word is made up of one or more basic instructions EI and at least one of instruction word delimiting fields 0 and 1. The basic instruction word length is either 1 or 2. 20 The upper row of FIG. 5 indicates an instruction word having a basic instruction word length of 2, consisting of a basic instruction word made up of an instruction word delimiting field 0 and a basic instruction EI, and another basic instruction word. 25 The upper row of FIG. 5 indicates an instruction word having a basic instruction word length of 2, consisting of a basic instruction word made up of an instruction word delimiting field 0 and a basic instruction EI, and another basic instruction word. 30 The upper row of FIG. 5 indicates an instruction word having a basic instruction word length of 1, consisting of an instruction word delimiting field 1 and a basic instruction EI. 35 The upper row of FIG. 5 indicates an instruction word having a basic instruction word length of 1, consisting of an instruction word delimiting field 1 and a basic instruction EI.

The above instruction words are stored in the memory 12 in advance. The adder 324 in the

instruction fetch unit 46 of the parallel processor 20 increments the address by a fixed length DISP, so that the instruction words can be fetched from the memory 12 in order. When the cutting unit 316 in 5 the instruction fetch unit 46 fetches the instruction word of the upper row of FIG. 5, for instance, it recognizes the instruction word delimiting field and the following basic instruction EI as one instruction word. The cutting unit 316 10 then cuts the instruction word from the instruction word string, and stores it in the instruction fetch unit 46. The adder 325 calculates the address corresponding to the basic instruction EI to be 15 executed in accordance with an instruction word length signal SL supplied from the cutting unit 316. The calculated address is temporarily stored in the EPC 339. A return address for rerunning the basic instruction EI that is stored in the EPC 339 is supplied to the register unit 98.

20 Based on the instruction word delimiting fields 0 and 1 contained in the instruction words supplied from the cutting unit 316, the instruction issue unit 72 recognizes each basic instruction EI, and issues each basic instruction EI selectively to 25 one of the instruction execution units EU0 and EU1 via the selectors 355 and 356. Accordingly, if a basic instruction EI following an instruction word delimiting field 0 is issued to the instruction execution unit EU0, while a basic instruction EI 30 following an instruction word delimiting field 1 is issued to the instruction execution unit EU1. The selectors 355 and 356 are controlled by the control unit 370. When the execution of one instruction word is completed, the corresponding basic 35 instruction EI is supplied to the instruction execution units EU0 and EU1 via the selectors 355 and 356.

Likewise, in a case where the instruction fetch unit 46 fetches and then supplies the instruction word having the basic instruction word length of 1 to the instruction buffer unit 308, the 5 cutting unit 316 cuts the basic instruction EI that follows the instruction word delimiting field 1 from the rest of the instruction word. The instruction register 347 then issues the basic instruction EI to one of the instruction execution units EU0 and EU1.

10 The instruction word delimiting fields 0 and 1 are both represented by one bit, but any sort of data can be written in those fields as long as they can function to delimit the instruction words. In this example, the two instruction execution units 15 EU0 and EU1 having the same structure are employed, but it is also possible to employ three or more instruction execution units.

20 As described so far, in the parallel processor 20 of this example, the instruction fetch unit 46 fetches instruction words one by one in accordance with the instruction word delimiting fields 0 and 1, so that the length of each of the instruction words can be made variable. The instruction issue unit 72 then issues a basic 25 instruction EI to a corresponding one of the instruction execution units EU0 and EU1.

30 Accordingly, there is no need to include do-nothing instructions NOP in any instruction word, and basic instructions EI can be efficiently included in each instruction word. By executing the basic instructions EI in the instruction words, the parallel processing performance of the parallel processor can be improved.

(Example 2)

35 FIG. 6 shows the structure of a second example of the parallel processor 21 in accordance with the first embodiment of the present invention.

As shown in FIG. 6, the parallel processor 21 has the same structure as the parallel processor 20 shown in FIG. 3, except for a judgment unit 103 that determines whether or not each basic instruction EI 5 supplied to the instruction issue unit 73 has data dependence or control dependence with a basic instruction EI being executed by one of the instruction execution units EU0 and EU1, and whether or not each basic instruction EI shares one resource 10 with another basic instruction EI being executed by one of the instruction execution units EU0 and EU1.

The judgment unit 103 compares a destination register number (write register number) defined in a basic instruction EI in execution with 15 a source register number (read register number) defined in a basic instruction EI to be issued to one of the instruction execution units EU0 and EU1. If the destination register number coincides with the source register number, it is confirmed that 20 there is data dependence between the two basic instructions EI. If the destination register number does not coincide with the source register number, it is confirmed that there is no data dependence between the two basic instructions EI, and the 25 operation can proceed.

The judgment unit 103 also determines whether or not the basic instruction EI in execution contains a branch instruction, and whether or not the basic instruction EI has a possibility of 30 starting an irregular process such as a division by 0. If the basic instruction EI in execution contains a branch instruction or has a possibility of an irregular process, there is control dependence between the basic instruction EI in execution and 35 the basic instruction EI to be issued to the instruction execution unit EU0 or EU1. If the basic instruction EI in execution neither contains a

096347-270000

branch instruction nor has a possibility of an irregular process, it is confirmed that there is no control dependency between the two basic instructions EI.

5 Based on the contents of each basic
instruction EI, the judgment unit 103 also compares
the resource (the instruction execution units EU0
and EU1, for instance) required by the basic
instruction EI in execution with the resource
10 required by the basic instruction EI to be issued.
If the resource required by the basic instruction EI
in execution is the same as the resource required by
the basic instruction EI to be issued, there is
resource sharing between the two basic instructions
15 EI. If the resources are different, it is confirmed
that there is no resource sharing between the two
basic instructions EI.

If the basic instruction EI to be issued has neither data dependency nor control dependency, and causes no resource sharing with the basic instruction EI being executed by the instruction execution units EU0 and EU1, the instruction issue unit 73 issues the basic instruction EI to a corresponding one of the instruction execution units EU0 and EU1 before the end of the execution. Here, the instruction issuance by the instruction issue unit 73 and the instruction execution by the instruction execution units EU0 and EU1 are processed by time-sharing parallel processing.

30 On the other hand, if the basic instruction EI to be issued has data dependency and/or control dependency, and/or causes resource sharing with the basic instruction EI being executed by the instruction execution units EU0 and EU1, the
35 basic instruction EI is issued to a corresponding one of the instruction execution units EU0 and EU1 after the end of the execution.

Although the two instruction execution units EU0 and EU1 having the same structure are employed in this example, it is also possible to employ three or more instruction execution units.

5 As described so far, the parallel processor 21 of this example can have the same effects as the parallel processor 20 of Example 1, and efficiently and accurately performs the parallel processing of the basic instructions EI. Thus, more
10 reliable operations can be achieved.

[Second Embodiment]

FIGS. 7, 12, 14, 16, 18, and 20 show parallel processors 22 to 27 in accordance with a
15 second embodiment of the present invention. Each of the parallel processors 22-27 comprises an instruction fetch unit 48-53 connected to a memory 12, an instruction issue unit 74-79 connected to the instruction fetch unit 48-53, instruction execution units LU0, IU0, IU1, FU0, FU1, and BU0 connected to the instruction issue unit 74-79, and a register unit 99 connected to all the instruction execution units LU0, IU0, IU1, FU0, FU1, and BU0.

20 The instruction execution unit LU0 is a load store instruction execution unit that executes a load instruction and a store instruction. After the execution of these instructions, the instruction execution unit LU0 notifies the instruction issue unit 74-79 of the end of the execution. The
25 instruction execution units IU0 and IU1 are integer arithmetic instruction execution units that execute integer arithmetic instructions. When the execution of the integer arithmetic instructions is completed, the instruction execution units IU0 and IU1 notify the instruction issue unit 74-79 of the end of the execution.
30
35

The instruction execution units FU0 and

FU1 are floating-point arithmetic instruction execution units that execute floating-point arithmetic instructions. When the execution of the floating-point arithmetic instructions is completed, 5 the instruction execution units FU0 and FU1 notify the instruction issue unit 74-79 of the end of the execution. The instruction execution unit BU0 is a branch instruction execution unit that executes a branch instruction. When the execution of the 10 branch instruction is completed, the instruction execution unit BU0 notifies the instruction issue unit 74-79 of the end of the execution.

In the following examples, the maximum basic instruction word length contained in one instruction word is 2, but the same effects can be expected in a case where the maximum basic instruction word length is 3 or greater.

(Example 1)

FIG. 7 shows the structure of a first example of the parallel processor in accordance with the second embodiment of the present invention. As shown in FIG. 7, the parallel processor 22 comprises a conversion unit 115 in the instruction fetch unit 48. The conversion unit 115 rearranges basic instructions contained in one fetched instruction word in accordance with the structure of the instruction execution units LU0, IU0, IU1, FU0, FU1, and BU0, and then supplies the rearranged basic instructions to the instruction issue unit 74. This rearrangement by the conversion unit 115 facilitates the issuance of the basic instructions of the instruction issue unit 74.

More specifically, the parallel processor of the present invention is embodied on a printed board or an LSI circuit. The components are arranged on a two-dimensional surface and connected by wires. At this point, the wires might cross each

other. However, a printed board and an LSI circuit have a plurality of wiring layers, so that any two wires that might cross each other can be arranged on two different wiring layers. Logically, it is 5 possible to place wires in any desired arrangement. In view of the operation speed of the circuit, however, the above alternate wiring (arranging wires on different wiring layers) requires longer wires, which will decrease the operation speed. Therefore, 10 it is preferable to have less alternate wiring. Shorter wires will facilitate the issuance of the basic instruction of the instruction issue unit 74, and increase the operation speed.

FIG. 8 shows the structures of the 15 instruction fetch unit 48 and the instruction issue unit 74 of the parallel processor 22 shown in FIG. 7. The instruction fetch unit 48 and the instruction issue unit 74 have the same structures as the instruction fetch unit 46 and the instruction issue 20 unit 72 shown in FIG. 4, except that the instruction fetch unit 48 includes the conversion unit 115 connected to a cutting unit 317. The instruction execution unit BU0 supplies information, such as a branch destination address corresponding to a branch 25 instruction, to a FPC 301.

For simplification of the drawing, only two instruction passages from an instruction register 348 to the two instruction execution units LU0 and LU1 are shown in FIG. 8. However, it should 30 be understood that there are other instruction passages to the instruction execution units IU1, FU0, FU1, and BU0, as shown in FIG. 7.

The parallel processor 22 of this example operates in the following manner. First, the 35 cutting unit 317 of the instruction fetch unit 48 fetches instruction words one by one. The formats 13 of the instruction words to be supplied to the

instruction fetch unit 48 are shown in FIG. 9. As shown in FIG. 9, each of the instruction words includes an instruction word delimiting field 0 and/or an instruction word delimiting field 1 and 5 one or two instructions selected from the group consisting of an integer arithmetic instruction II, a floating-point arithmetic instruction FI, a load store instruction LI, and a branch instruction BI.

An interface 15 for the instruction 10 execution units LU0, IU0, IU1, FU0, FU1 and BU0, includes effective bits V, information II required for executing an integer arithmetic instruction, information FI required for executing a floating-point arithmetic instruction, information LI 15 required for executing a load store instruction, and information BI required for executing a branch instruction. The interface 15 supplies the effective bit V and the information LI from the instruction issue unit 74 to the instruction 20 execution unit LU0, the effective bit V and the information II to the instruction execution units IU0 and IU1, the effective bit V and the information FI to the instruction execution units FU0 and FU1, and the effective bit V and the information BI to 25 the instruction execution unit BU0.

When the effective bit V is 0, no basic instruction is issued, and when the effective bit 1, a basic instruction is issued. Each effective bit V is coupled with the information II, FI, LI, or BI, 30 and is then allocated to each corresponding instruction execution unit.

As shown in FIG. 9, the instruction word formats 13 are rearranged and converted into instruction word formats 17 by the conversion unit 35 115 in the instruction fetch unit 48. The instruction word formats 17 correspond to the instruction execution units LU0, IU0, IU1, FU0, FU1,

and BU0, and are supplied to the instruction register 348 in the instruction issue unit 74. The instruction register 348 issues basic instructions each having the effective bit V of 1 to 5 corresponding instruction execution units. For instance, when the instruction word on the uppermost row of the instruction word format 17 is supplied to the instruction issue unit 74, the instruction issue unit 74 issues the floating-point arithmetic 10 instruction FI provided with "1" as the effective bit V to the instruction execution unit FU0, and the branch instruction BI also provided with "1" as the effective bit V to the instruction execution unit BU0.

15 As a result, the instruction execution unit FU0 executes the floating-point arithmetic instruction FI, and the instruction execution unit BU0 executes the branch instruction BI. In this case, no basic instructions are executed by the 20 other instruction execution units LU0, IU0, IU1, and FU1.

FIG. 10 is a circuit diagram of the conversion unit 115 shown in FIG. 8. As shown in FIG. 10, the conversion unit 115 comprises 25 transmission lines L1 and L2, BI detectors BD1 and BD2, FI detectors FD1 and FD2, II detectors ID1 and ID2, LI detectors LD1 and LD2, buffers 155 to 158, AND gates 163 to 166, 185, and 186, exclusive OR gates 187 to 190, selectors 209 to 212, and OR gates 30 199 to 202.

The transmission line L1 transmits the first basic instruction contained in each instruction word, and the transmission line L2 transmits the second basic instruction contained in 35 each instruction word. The BI detector BD1 is connected to the transmission line L1, and the BI detector BD2 is connected to the transmission line

L2. The buffer 155 is connected to the BI detector BD1, and the AND gate 163 is connected to the BI detectors BD1 and BD2. The selector 209 is connected to the transmission lines L1 and L2, the buffer 155, and the AND gate 163. The OR gate 199 is connected to the buffer 155 and the AND gate 163.

The FI detector FD1 is connected to the transmission line L1, and the FI detector FD2 is connected to the transmission line L2. The buffer 156 is connected to the FI detector FD1, and the AND gate 164 is connected to the FI detectors FD1 and FD2. The two input terminals of the exclusive OR gate 187 are connected to the input node and the output node, respectively, of the buffer 156. The two input terminals of the exclusive OR gate 188 are connected to the output node of the AND gate 164 and the FI detector FD2, respectively. The AND gate 185 is connected to the two exclusive OR gates 187 and 188. The selector 210 is connected to the transmission lines L1 and L2, the buffer 156, and the AND gate 164. The OR gate 200 is connected to the buffer 156 and the AND gate 164.

25 The II detector ID1 is connected to the transmission line L1, and the II detector ID2 is connected to the transmission line L2. The buffer 157 is connected to the II detector ID1, and the AND gate 165 is connected to the II detectors ID1 and ID2. The two input terminals of the exclusive OR gate 189 are connected to the input node and the 30 output node, respectively, to the buffer 157. The two input terminals of the exclusive OR gate 190 are connected to the output node of the AND gate 165 and the II detector ID2, respectively. The AND gate 186 is connected to the two exclusive OR gates 189 and 35 190. The selector 211 is connected to the transmission lines L1 and L2, the buffer 157, and the AND gate 165. The OR gate 201 is connected to

the buffer 157 and the AND gate 165.

The LI detector LD1 is connected to the transmission line L1, and the LI detector LD2 is connected to the transmission line L2. The buffer 158 is connected to the LI detector LD1, and the AND gate 166 is connected to the LI detectors LD1 and LD2. The selector 212 is connected to the transmission lines L1 and L2, the buffer 158, and the AND gate 166. The OR gate 202 is connected to the buffer 158 and the AND gate 166.

The two BI detectors BD1 and BD2 constitute a BI detector block 147. The two FI detectors FD1 and F2 constitute an FI detector block 149. The two II detectors ID1 and ID2 constitute an II detector block 151. The two LI detectors LD1 and LD2 constitute an LI detector block 153.

In the following, an operation of the conversion unit 115 having the above structure will be described by way of an example case where the instruction word including the basic instructions BI and FI on the uppermost row of the instruction word formats 13 shown in FIG. 9 is supplied to the conversion unit 115. First, the basic instruction BI is transmitted through the transmission line L1. The BI detector BD1 then detects the basic instruction BI and supplies a detection signal of logic 1 to the buffer 155. At this point, the AND gate 163 outputs a logic 0 signal. In accordance with the detection signal supplied from the buffer 155, the selector 209 selects the first basic instruction BI and outputs the first basic instruction BI, that is, an instruction to be executed by the instruction execution unit BU0, to the instruction issue unit 74. At the same time as the output of the basic instruction BI, in accordance with the detection signal supplied from the buffer 155, the OR gate 199 outputs the

effective bit V of logic 1. As the first basic instruction BI is detected, the FI detector FD1, the II detector ID1, and the LI detector LD1 output non-detection signals of logic 0. Accordingly, the 5 selectors 210, 211, and 212 do not select the first basic instruction transmitted through the transmission line L1.

Next, the second basic instruction FI in the instruction word is transmitted through the 10 transmission line L2. As in the case of the first basic instruction BI, The FI detector FD2 detects the second basic instruction FI and supplies a detection signal of logic 1 to the AND gate 164. The AND gate 164 in turn outputs a logic 1 signal. 15 In accordance with the logic 1 signal supplied from the AND gate 164, the selector 210 selects the second basic instruction FI and outputs the second basic instruction FI as an instruction to be executed by the instruction execution unit FU0. At 20 the same time as the output of the basic instruction FI, the OR gate 200 outputs the effective bit V of logic 1 in accordance with the detection signal supplied from the AND gate 164.

As the second basic instruction FI is 25 detected, the BI detector BD2, the II detector ID2, and the LI detector LD2 output non-detection signals of logic 0. Accordingly, the selectors 209, 211, and 212 do not select the second basic instruction transmitted through the transmission line L2. Since 30 neither first nor second basic instructions to be executed by the instruction executed units LU0, IU0, IU1, and FU1 are detected, the effective bet V of logic 0 is outputted from each of the OR gates 201 and 202, and the AND gates 185 and 186.

35 In the above described manner, the conversion unit 115 converts the instruction word formats 13 into the instruction word formats 17, as

shown in FIG. 9.

FIG. 11 is a circuit diagram of the conversion unit 115 in a case where the maximum basic instruction word length of one instruction word to be supplied from the memory 12 to the instruction fetch unit 48 is 4. As shown in FIG. 11, the structure of the conversion unit 115 in this case is the same as the structure of the conversion unit 115 shown in FIG. 10, except that the number of transmission lines are 4, the number of BI detectors is 4, the number of FI detectors is 4, the number of II detectors is 4, and the number of LI detectors is 4. Also, two selectors 214 and 215 are provided for a basic instruction FI, and two selectors 216 and 217 are provided for a basic instruction II in this case.

The conversion unit 115 further includes buffers 159 to 162, AND gates 167 to 184, exclusive OR gates 191 to 198, OR gates 203 to 208, and 20 selectors 213 and 218. The four BI detectors BD1 to BD4 constitute a BI detector block 148. The four FI detectors FD1 to FD4 constitute an FI detector block 150. The four II detectors ID1 to ID4 constitute an ID detector block 152. The four LI detectors LD1 to 25 LD4 constitute an LI detector block 154.

The conversion unit 115 having the above structure operates in the same manner as the conversion unit 115 shown in FIG. 10. In the following, an operation of the conversion unit 115 30 in a case where an instruction word made up of basic instructions BI, FI, FI, and II is supplied to the conversion unit 115 will be described. First, the first basic instruction BI is transmitted through the transmission line L1. The BI detector BD1 then 35 detects the basic instruction BI and supplies a detection signal of logic 1 to the buffer 159. At this point, each of the AND gates 167 to 169 outputs

a logic 0 signal. In accordance with the detection signal supplied from the buffer 159, the selector 213 selects the first basic instruction BI and outputs the first basic instruction BI, that is an 5 instruction to be executed by the instruction execution unit BU0, to the instruction issue unit 74. At the same time as the output of the first basic instruction BI, the OR gates 203 outputs the effective bit V of logic 1 in accordance with the 10 detection signal supplied from the buffer 159. As the first basic instruction BI is detected, the FI detector FD1, the II detector ID1, and the LI detector LD1 output non-detection signal of logic 0. Accordingly, the selectors 214, 216, and 218 do not 15 select the first basic instruction BI transmitted through the transmission line L1.

Next, the second basic instruction FI is transmitted on the transmission line L2. The FI detector FD2 then detects the second basic 20 instruction FI and supplies a detection signal of logic 1 to the AND gate 170. The AND gate 170 in turn outputs a logic 1 signal. In accordance with the logic 1 signal supplied from the AND gate 170, the selector 214 selects the second basic 25 instruction FI and outputs the second basic instruction FI as an instruction to be executed by the instruction execution unit FU0. At the same time as the output of the second basic instruction FI, the OR gate 204 outputs the effective bit V of logic 1 in accordance with the detection signal 30 supplied from the AND gate 170.

As the second basic instruction FI is detected, the BI detector BD2, the II detector ID2, and the LI detector LD2 each output a non-detection 35 signal of logic 0. Accordingly, the selectors 213, 216, and 218 do not select the second basic instruction FI transmitted through the transmission

0010001000000000

line L2.

Next, the third basic instruction FI is transmitted through the transmission line L3. The FI detector FD3 then detects the third basic instruction FI and supplies a detection signal of logic level 1 to the AND gate 171. Since the AND gate 171 has already received a detection signal of logic 1 from the FI detector FD2 at this point, the output of the AND gate 171 is a logic 0 signal.

Because of that, the exclusive OR gate 193 outputs a logic 1 signal, and the AND gate 174 also outputs a logic 1 signal. In accordance with the logic 1 signal supplied from the AND gate 174, the selector 215 selects the third basic instruction FI and outputs the third basic instruction FI as an instruction to be executed by the instruction execution unit FU1. At the same time as the output of the third basic instruction FI, the OR gate 205 outputs the effective bit V of logic 1 in accordance with the signal supplied from the AND gate 174.

As the third basic instruction FI is detected, the BI detector BD3, the II detector ID3, and the LI detector LD3 each output a non-detection signal of logic 0. Accordingly, the selectors 213, 216, and 218 do not select the third basic instruction FI transmitted through the transmission line 3.

30 Next, the fourth basic instruction II of the instruction word is transmitted through the transmission line L4. The II detector ID4 then detects the fourth basic instruction II and supplies a detection signal of logic 1 to the AND gate 178. The AND gate 178 in turn outputs a logic 1 signal. In accordance with the logic 1 signal supplied from 35 the AND gate 178, the selector 216 selects the fourth basic instruction II and outputs the fourth basic instruction II as an instruction to be

executed by the instruction execution unit IU0. At the same time as the output of the fourth basic instruction II, the OR gate 206 outputs the effective bit V of logic 1 in accordance with the signal supplied from the AND gate 178.

As described above, in the parallel processor of this example, basic instructions contained in each instruction word supplied to the instruction fetch unit 48 are rearranged in accordance with the arrangement of the instruction execution units, so that the instruction issue unit 74 can smoothly issue the basic instructions to the respective instruction execution units. Thus, the entire operation speed can be increased.

15 In this example, the instruction fetch
unit 48 can also fetch an instruction word
containing basic instructions that have already been
arranged in accordance with the arrangement of the
instruction execution units in advance. In such a
20 case, the basic instruction are arranged in advance
so that the circuit size required for rearranging
the basic instructions in the instruction fetch unit
48 can be reduced.

More specifically, when there are two
25 instructions for the same function, only one of the
two instructions is employed. For instance, the
instruction word on the uppermost row and the
instruction word on the fourth row from the top of
the formats 13 in FIG. 9 are rearranged into the
30 same formats in the formats 17. In this case, only
one of the two instruction words should be employed,
while the use of the other should be inhibited.
Alternatively, an instruction word that will
increase the number of alternate wire routes in the
35 instruction fetch unit 48 may be inhibited
beforehand. For instance, the instruction words on
the upper most row and the fourth row from the top

of the formats 13 in FIG. 9 have the basic instructions BI and FI in the opposite orders. Since the circuit components are arranged on a two-dimensional surface, one of the two basic 5 instructions requires more alternate wire routes than the other. Accordingly, the instruction word that requires more alternate wire routes should be inhibited in advance.

As described so far, the circuit size of 10 the parallel processor 22 can be reduced by restricting in advance the arrangement of basic instruction contained in each instruction word to be supplied to the instruction fetch unit 48.

(Example 2)

15 FIG. 12 shows the structure of a second example of the parallel processor in accordance with the second embodiment of the present invention. As shown in FIG. 12, the parallel processor 23 of this example has the same structure as the parallel 20 processor 22 of Example 1, except that a conversion unit 116 is included in the instruction issue unit 75. The conversion unit 116 has the same structure and functions as the conversion unit 115 shown in FIGS. 10 and 11.

25 FIG. 13 shows the structures of the instruction fetch unit 49 and the instruction issue unit 75 of the parallel processor 23 shown in FIG. 12. The instruction fetch unit 49 and the instruction issue unit 75 has the same structures as 30 the instruction fetch unit 46 and the instruction issue unit 72 shown in FIG. 4, except that the instruction issue unit 75 includes the conversion unit 116 connected to an instruction register 349. For simplification of the drawing, only the 35 instruction passages to the two instruction execution units LU0 and IU0 are shown, and the instruction passages to the other instruction

001060-225455600

execution units IU1, FU0, FU1, and BU0 are omitted in FIG. 13. Also, only two execution complete signals LUC and IUC0 to be supplied to the AND gate 380 are shown, and the other execution complete 5 signals are omitted in FIG. 13.

With the parallel processor of this example, basic instructions contained in each instruction word supplied from the instruction register 349 are rearranged by the conversion unit 116 in accordance with the arrangement of the 10 instruction execution units. The rearranged basic instructions are then issued to the corresponding instruction execution units. Thus, the wires can be shortened as a whole, and the operation speed can be 15 increased.

Also, the arrangement of basic instruction contained in each instruction word to be supplied to the instruction fetch unit 49 can be restricted in advance in the same manner as in Example 1. Thus, 20 the circuit size of the parallel processor 23 can be reduced.

(Example 3)

FIG. 14 shows the structure of a third example of the parallel processor in accordance with 25 the second embodiment of the present invention. As shown in FIG. 14, the parallel processor 24 has the same structure as the parallel processor 22 of Example 1 shown in FIG. 7, except that the instruction fetch unit 50 includes a first 30 conversion unit 117 and the instruction issue unit 76 includes a second conversion unit 118. The first conversion unit 117 rearranges basic instructions contained in each instruction word in accordance with the arrangement of the instruction execution 35 units. The second conversion unit 118 rearranges basic instructions contained in each instruction word in accordance with the arrangement of the

instruction execution units.

FIG. 15 shows the structures of the instruction fetch unit 50 and the instruction issue unit 76 of the parallel processor unit 24 shown in FIG. 14. The instruction fetch unit 50 and the instruction issue unit 76 have the same structures as the instruction fetch unit 46 and the instruction issue unit 72 shown in FIG. 4, except that the instruction fetch unit 50 further includes the first conversion unit 117 connected to a cutting unit 319 and the instruction issue unit 76 further includes the second conversion unit 118 connected to an instruction register 350. For simplification of the drawing, only the instruction passages from the second conversion unit 118 to the two instruction execution units LU0 and IU0 are shown, and the instruction passages to the other instruction execution units IU1, FU0, FU1, and BU0 are omitted in FIG. 15. Likewise, only two execution complete signals LUC and IUC0 to be supplied to the AND gate 381 are shown, and the other execution complete signals are omitted in FIG. 15.

25 The first conversion unit 117 performs "preprocessing" of the rearrangement of basic instructions. The second conversion unit 118 performs "postprocessing" of the rearrangement of basic instructions.

In an actual circuit, the processes performed by the instruction fetch unit 50 and the instruction issue unit 76 are pipelined so as to improve the performance of the parallel processor. Because of that, the difference in processing time between instruction fetch unit 50 and the instruction issue unit 76 should be as small as possible to optimize the pipeline effects. Therefore, the arrangement process is divided into the "preprocessing" and "postprocessing", so that

the difference in processing time between the instruction fetch unit 50 and the instruction issue unit 76 is small.

More specifically, the first conversion unit 117 includes circuits that are the counterparts of the BI detector block 147 or 148, the FI detector block 149 or 150, the II detector block 151 or 152, and the LI detector block 153 or 154 shown in FIGS. 10 and 11. The other circuits shown in FIGS. 10 and 11 are included in the second conversion unit 118.

With the parallel processor 24 having the above structure, the wires can be shortened as a whole, and the operation speed can be reduced.

Also, as in Examples 1 and 2, the circuit size of the parallel processor 24 may be reduced by restricting in advance the arrangement of basic instructions contained in each instruction word to be supplied to the instruction fetch unit 50.

(Example 4)

FIG. 16 shows the structure of a fourth example of the parallel processor in accordance with the second embodiment of the present invention. As shown in FIG. 16, the parallel processor 25 has the same structure as the parallel processor 22 of Example 1 shown in FIG. 7, except that the instruction fetch unit 51 includes a conversion unit 119 and the instruction issue unit 77 includes a judgment unit 104.

FIG. 17 shows the structures of the instruction fetch unit 51 and the instruction issue unit 77 of the parallel processor 25 shown in FIG. 16. The instruction fetch unit 51 and the instruction issue unit 77 have the same structures as the instruction fetch unit 48 and the instruction issue unit 74 shown in FIG. 8, except that the instruction issue unit 77 further includes the judgment unit 104. The judgment unit 104 determines

whether or not a basic instruction to be issued has data dependency or control dependency with a supplied basic instruction. The judgment unit 104 also determines whether or not the basic instruction 5 to be issued shares resources with the supplied basic instruction. If the basic instruction to be issued has data dependency or control dependency, or shares resources with the supplied basic instruction, the instruction issue unit 77 issues the basic 10 instruction after the execution complete signals LUC and IUC0 are supplied.

For simplification of the drawing, only the instruction passages from an instruction register 351 to the two instruction execution units 15 LU0 and IU0 are shown, and the other instruction passages to the instruction execution units IU1, FU0, FU1, and BU0 are omitted in FIG. 17. Likewise, only the two execution complete signals LUC and IUC0 are shown as signals to be supplied to the judgment unit 20 104, but the other execution complete signals are omitted in FIG. 17.

The structure and operation of the conversion unit 119 are substantially the same as the structure and operation of the conversion unit 25 15 shown in FIGS. 10 and 11. The structure and operation of the judgment unit 104 are substantially the same as the structure and operation of the judgment unit 103 shown in FIG. 6.

By the parallel processor of this example 30 having the above structure, the same effects as obtained by the parallel processor of Example 2 of the first embodiment and the parallel processor of Example 1 of the second embodiment can be obtained. In the parallel processor of this example, the 35 instruction issue unit 77, which includes the judgment unit 104, enables accurate and efficient parallel processing of basic instructions, thereby

increasing the reliability of the parallel processor. Also, the instruction fetch unit 51, which includes the conversion unit 119, facilitates the basic instruction issuance to the instruction execution units by the instruction issue unit 77, thereby increasing the operation speed.

As in the foregoing examples, the circuit size of the parallel processor 25 may be reduced by restricting in advance the arrangement of basic instructions contained in each instruction word to be supplied to the instruction fetch unit 51.

(Example 5)

15 FIG. 18 shows the structure of a fifth example of the parallel processor in accordance with the second embodiment of the present invention. As shown in FIG. 18, the parallel processor 26 has the same structure as the parallel processor 25 of Example 4, except that the instruction fetch unit 52 includes no conversion unit and the instruction 20 issue unit 78 further includes a conversion unit 120.

FIG. 19 shows the structures of the instruction fetch unit 52 and the instruction issue unit 78 of the parallel processor 26 shown in FIG. 18. The instruction fetch unit 52 and the instruction issue unit 78 have the same structures as the instruction fetch unit 49 and the instruction issue unit 75 shown in FIG. 13, except that the instruction issue unit 78 further includes the judgment unit 105 connected between an instruction register 352 and a control unit 375. In accordance with a supplied basic instruction, the judgment unit 105 determines whether or not a basic instruction to be issued has the data dependency or control dependency, and whether or not the basic instruction to be issued will cause resource sharing. The judgment results are reported to the control unit 375. If the basic instruction to be issued has the

data dependency or control dependency, or causes resource sharing, the issue instruction unit 78 issues the basic instruction after the supply of the execution complete signals LUC and IUC0.

5 For simplification of the drawing, only the instruction passages from the instruction register 352 to the two instruction execution units LU0 and IU0 are shown, and the instruction passages to the other instruction execution units are omitted
10 10 in FIG. 19. Likewise, only the two execution complete signals LUC and IUC0 to be supplied to the judgment unit 105 are shown in FIG. 19.

15 The structure and operation of the conversion unit 120 are the same as the structure and operation of the conversion unit 115 shown in FIGS. 10 and 11. The structure and operation of the judgment unit 105 are the same as the structure and operation of the judgment unit 104 shown in FIG. 16.

20 The parallel processor of this example having the above structure achieves the same effects as the parallel processor of Example 4. The instruction issue unit 78 including the judgment unit 105 enables accurate and efficient parallel processing of basic instructions, thereby increasing
25 the reliability of the operation. Also, the instruction issue unit 78, which further includes the conversion unit 120, facilitates the issuance of basic instructions to the instruction execution units.

30 Additionally, the circuit size of the parallel processor 26 may be reduced by restricting in advance the arrangement of basic instructions contained in each instruction word to be supplied to the instruction fetch unit 52, as in the foregoing
35 examples.

(Example 6)

FIG. 20 shows the structure of a sixth

example of the parallel processor in accordance with the second embodiment of the present invention. As shown in FIG. 20, the parallel processor 27 has the same structure as the parallel processor 24 of 5 Example 3 shown in FIG. 14, except that the instruction issue unit 79 further includes a judgment unit 106.

FIG. 21 shows the structures of the instruction fetch unit 53 and the instruction issue 10 unit 79 of the parallel processor 27 shown in FIG. 20. The instruction fetch unit 53 and the instruction issue unit 79 have the same structures as the instruction fetch unit 50 and the instruction issue unit 76 shown in FIG. 15, except that the 15 instruction issue unit 79 further includes the judgment unit 106 connected between an instruction register 353 and a control unit 376. Based on a supplied basic instruction, the judgment unit 106 determines whether or not a basic instruction to be 20 issued has the data dependency or control dependency, or causes resource sharing. The judgment results area reported to the control unit 376. If the basic instruction to be issued has the data dependency or control dependency, or causes resource sharing, the 25 instruction issue unit 79 issues the basic instruction only after the execution complete signals L_{Uc} and I_{Uc0} are supplied.

For simplification of the drawing, only the instruction passages from the instruction 30 register 353 to the two instruction execution units LU0 and IU0 are shown, and the instruction passages to the other instruction execution units IU1, FU0, FU1, and BU0 are omitted in FIG. 21. Likewise, only the two execution complete signals L_{Uc} and I_{Uc0} are 35 shown in FIG. 21.

The structures and operations of a first conversion unit 121 and a second conversion unit 122

are the same as the structures and operations of the first conversion unit 117 and the second conversion unit 118. The structure and operation of the judgment unit 106 are the same as the structure and 5 operation of the judgment unit 103 shown in FIG. 6.

The parallel processor 27 of this example having the above structure can achieve both effects of the parallel processor of Example 2 of the first embodiment and the parallel processor of Example 3 10 of the second embodiment. More specifically, the instruction issue unit 79 including the judgment unit 106 enables accurate and efficient parallel processing of basic instructions, thereby increasing the reliability of the operation. Also, the 15 instruction fetch unit 53 including the first conversion unit 121 and the instruction issue unit 79 including the second conversion unit 122 facilitate the issuance of basic instructions from the instruction issue unit 79 to the instruction 20 execution units.

Additionally, the circuit size of the parallel processor 27 may be reduced by restricting in advance the arrangement of basic instructions contained in each instruction word to be supplied to 25 the instruction fetch unit 53, as in the foregoing examples.

[Third Embodiment]

As shown in FIGS. 22 to 27, parallel 30 processors 28 to 33 in accordance with a third embodiment of the present invention each comprises an instruction fetch unit 54-59 connected to the memory 12, an instruction issue unit 80-85 connected to the instruction fetch unit 54-59, instruction 35 execution units LU0, IU0, IU1, FU0, FU1, MU0, MU1, and BU0, and a register unit 100 connected to all the instruction execution units. Here, the

instruction execution units MU0 and MU1 are special-purpose arithmetic instruction execution units that execute special-purpose arithmetic instructions. When the execution of special-purpose arithmetic 5 instructions is completed, the instruction execution units MU0 and MU1 notify the instruction issue unit 80-85 of the complete of the execution.

In the following, the parallel processors in accordance with the third embodiment of the 10 present invention will be described by way of a case where the maximum basic instruction word length contained in one instruction word is 2. It should be understood that the same effects can be obtained in a case where the maximum instruction word length 15 contained in one instruction word is 3 more greater.

(Example 1)

FIG. 22 shows the structure of a first example of the parallel processor in accordance with the third embodiment of the present invention. As 20 shown in FIG. 22, the parallel processor 28 comprises a conversion unit 123 in the instruction fetch unit 54. The structure and the operation of the conversion unit 123 are the same as the conversion unit 115 of Example 1 of the second 25 embodiment. More specifically, the conversion unit 123 rearranges basic instructions contained in each instruction word in accordance with the arrangement of the instruction execution units, and then supplies the rearranged basic instructions to the 30 instruction issue unit 80.

The parallel processor 28 having the above structure can achieve the same effects as the parallel processor 22 of Example 1 of the second embodiment. In other words, the issuance of basic 35 instructions from the instruction issue unit 80 to the instruction execution units can be facilitated, and the operation speed can be increased.

Additionally, the circuit size of the parallel processor 28 may be reduced by restricting in advance the arrangement of basic instructions contained in each instruction word to be supplied to 5 the instruction execution units, as in the foregoing examples.

(Example 2)

FIG. 23 shows the structure of a second example of the parallel processor in accordance with 10 the third embodiment of the present invention. As shown in FIG. 23, the parallel processor 29 has the same structure as the parallel processor 23 shown in FIG. 12, comprising a conversion unit 124 in the instruction issue unit 81. The structure and 15 operation of the conversion unit 124 are the same as the structure and operation of the conversion unit 115 shown in FIGS. 10 and 11.

In the parallel processor 29 of this example, the instruction issue unit 81 issues each 20 basic instruction to the corresponding one of the instruction execution units, only after the conversion unit 124 rearranges the basic 25 instructions, which are contained in each instruction word supplied from the instruction fetch unit 55, in accordance with the arrangement of the instruction execution units. Thus, wires can be shortened as a whole, and the operation speed can be increased.

Additionally, the circuit size of the 30 parallel processor 29 may be reduced by restricting in advance the arrangement of basic instructions contained in each instruction word to be supplied to the instruction fetch unit 55, as in the foregoing examples.

35 (Example 3)

FIG. 24 shows the structure of a third example of the parallel processor in accordance with

the third embodiment of the present invention. As shown in FIG. 24, the parallel processor 30 has substantially the same structure as the parallel processor 24 shown in FIG. 14. The instruction 5 fetch unit 56 includes a first conversion unit 125 that rearranges basic instructions contained in each fetched instruction word in accordance with the arrangement of the instruction execution units. The instruction issue unit 82 includes a second 10 conversion unit 126 that further rearranges basic instructions contained in each instruction word supplied from the instruction fetch unit 56 in accordance with the arrangement of the instruction execution units.

15 The first conversion unit 125 performs "preprocessing" of rearrangement of basic instructions, and the second conversion unit 126 performs "postprocessing" of basic instructions.

20 In an actual circuit, the processes in the instruction fetch unit 56 and the instruction issue unit 82 are pipelined in order to improve the performance of the parallel processor. Because of that, the difference in processing time between 25 instruction fetch unit 56 and the instruction issue unit 82 should be as small as possible to optimize the pipeline effects. Therefore, the arrangement process is divided into the "preprocessing" and "postprocessing", so that the difference in processing time between the instruction fetch unit 30 56 and the instruction issue unit 82 is small.

By the parallel processor of this example having the above structure, wires can be shortened as a whole, and the operation speed can be increased.

35 Additionally, the circuit size of the parallel processor 30 may be reduced by restricting in advance the arrangement of basic instructions contained in each instruction word to be supplied to

09534523 090100

the instruction fetch unit 56, as in the foregoing examples.

(Example 4)

FIG. 25 shows the structure of a fourth embodiment of the parallel processor in accordance with the third embodiment of the present invention. As shown in FIG. 25, the parallel processor 31 has the same structure as the parallel processor 25 shown in FIG. 16. The instruction fetch unit 57 includes a conversion unit 127, and the instruction issue unit 83 includes a judgment unit 107.

The structure and operation of the conversion unit 127 are the same as the structure and operation of the conversion unit 115 shown in FIGS. 10 and 11. The structure and operation of the judgment unit 107 are the same as the structure and operation of the judgment unit 103 shown in FIG. 6.

By the parallel processor of this example having the above structure, the same effects as the parallel processor of Example 4 of the second embodiment can be obtained. More specifically, the instruction issue unit 83 including the judgment unit 107 enables accurate and efficient parallel processing of basic instructions, thereby increasing the reliability of the operation. The instruction fetch unit 57 including the conversion unit 127 facilitates the issuance of basic instructions to the instruction execution units, thereby increasing the operation speed.

30 Additionally, the circuit size of the parallel processor 31 may be reduced by restricting in advance the arrangement of basic instructions contained in each instruction word to be supplied to the instruction fetch unit 57, as in the foregoing 35 examples.

(Example 5)

FIG. 26 shows the structure of a fifth

example of the parallel processor in accordance with the third embodiment of the present invention. As shown in FIG. 26, the parallel processor 32 has the same structure as the parallel processor 26 of 5 Example 5 of the second embodiment shown in FIG. 18. The instruction issue unit 84 includes a conversion unit 128 and a judgment unit 108.

The structure and operation of the conversion unit 128 are the same as the structure 10 and operation of the conversion unit 115 shown in FIGS. 10 and 11. The structure and operation of the judgement unit 108 are the same as the structure and operation of the judgment unit 103.

By the parallel processor of this example 15 having the above structure, the same effects as the parallel processor 26 of Example 5 of the second embodiment. More specifically, the instruction issue unit 84 including the judgment unit 108 enables accurate and efficient parallel processing 20 of basic instructions, thereby increasing the reliability of the operation. The instruction issue unit 84 further including the conversion unit 128 facilitates the issuance of basic instructions to the instruction execution units, thereby increasing 25 the operation speed.

Additionally, the circuit size of the parallel processor 32 may be reduced by restricting in advance the arrangement of basic instructions contained in each instruction word to be supplied to 30 the instruction fetch unit 58, as in the foregoing examples.

(Example 6)

FIG. 27 shows the structure of a sixth example of the parallel processor in accordance with 35 the third embodiment of the present invention. As shown in FIG. 27, the parallel processor 33 has the same structure as the parallel processor 27 as shown

in FIG. 20.

The structures and operations of a first conversion unit 129 and a second conversion unit 130 are the same as the structures and operations of the 5 first conversion unit 117 and the second conversion unit 118 shown in FIG. 14. The structure and operation of a judgment unit 109 are the same as the structure and operation of the judgment unit 103.

By the parallel processor of this example 10 having the above structure, the same effects as obtained by the parallel processor 27 of Example 6 of the second embodiment can be obtained. More specifically, the instruction issue unit 85 including the judgment unit 109 enables accurate and 15 efficient parallel processing of basic instructions, thereby increasing the reliability of the operation. The instruction fetch unit 59 including the first conversion unit 129 and the instruction issue unit 85 including the second conversion unit 130 20 facilitate the issuance of basic instructions from the instruction issue unit 85 to the instruction execution units, thereby increasing the operation speed.

Additionally, the circuit size of the 25 parallel processor 33 may be reduced by restricting in advance the arrangement of basic instructions contained in each instruction word to be supplied to the instruction fetch unit 59, as in the foregoing examples.

30

[Fourth Embodiment]

As shown in FIGS. 28 to 33, a parallel processor 34-39 in accordance with a fourth embodiment of the present invention each comprises 35 an instruction fetch unit 60-65 connected to the memory 12, an instruction issue unit 86-91 connected to the instruction fetch unit 60-65, instruction

execution units LU0, LU1, IU0, IU1, FU0, FU1, BU0, and BU1 connected to the instruction issue unit 86-91, and a register unit 101 connected to all the instruction execution units. In this embodiment, 5 the instruction execution unit LU1 is a load store instruction execution unit that executes load instructions and store instructions. The instruction execution unit BU1 is a branch instruction execution unit that executes branch 10 instructions. When the execution is completed, the instruction execution unit BU1 notifies the instruction issue unit 86-91 of the end of the execution.

In the following, the parallel processor 15 in accordance with the fourth embodiment of the present invention will be described by way of examples in which the maximum basic instruction word length contained in each one basic instruction is 4. In FIGS. 28 to 33, the maximum basic instruction 20 word length being 4 is indicated by four arrows from the instruction fetch unit 60-65 to the instruction issue unit 86-91. However, it should be understood that the maximum basic instruction word length in the fourth embodiment is not limited to 4.

25 (Example 1)

FIG. 28 shows the structure of a first example of the parallel processor in accordance with the fourth embodiment of the present invention. As shown in FIG. 28, the parallel processor 34 30 comprises a conversion unit 131 in the instruction fetch unit 60. The structure and operation of the conversion unit 131 are the same as the structure and operation of the conversion unit 115 of Example 1 of the second embodiment. More specifically, the 35 conversion unit 131 rearranges basic instructions contained in each fetched instruction word, in accordance with the arrangement of the instruction

execution units, and supplies the rearranged basic instructions to the instruction issue unit 86.

By the parallel processor 34 having the above structure, the same effects as obtained by the parallel processor 22 of Example 1 of the second embodiment can also be obtained. More specifically, the issuance of basic instructions from the instruction issue unit 86 to the instruction execution units can be facilitated, and the operation speed can be increased accordingly.

15 Additionally, the circuit size of the parallel processor 34 may be reduced by restricting in advance the arrangement of basic instructions contained in each instruction word to be supplied to the instruction fetch unit 60, as in the foregoing embodiments.

(Example 2)

FIG. 29 shows the structure of a second example of the parallel processor in accordance with the fourth embodiment of the present invention. As shown in FIG. 29, the parallel processor 35 has the same structure as the parallel processor 23 shown in FIG. 12, in that the instruction issue unit 87 includes a conversion unit 132. The structure and operation of the conversion unit 132 are the same as the structure and operation of the conversion unit 115 shown in FIGS. 10 and 11.

In the parallel processor 35 of this example, the instruction issue unit 87 rearranges 30 basic instructions contained in each instruction word supplied to the instruction fetch unit 61, in accordance with the arrangement of the instruction execution unit, and then supplies the rearranged basic instructions to the instruction execution 35 units. Thus, wires can be shortened as a whole, and the operation speed can be increased.

Additionally, the circuit size of the

parallel processor 35 may be reduced by restricting in advance the arrangement of basic instructions contained in each instruction word to be supplied to the instruction fetch unit 61, as in the foregoing examples.

(Example 3)

FIG. 30 shows the structure of a third example of the parallel processor in accordance with the fourth embodiment of the present invention. As shown in FIG. 30, the parallel processor 36 has the same structure as the parallel processor 24 shown in FIG. 14. The instruction fetch unit 62 of this parallel processor 36 includes a first conversion unit 133 that rearranges basic instructions contained in each fetched instruction word, in accordance with the arrangement of the instruction execution units. The instruction issue unit 88 of the parallel processor 36 includes a second conversion unit 134 that further rearranges the basic instructions contained in each instruction word supplied from the instruction fetch unit 62, in accordance with the arrangement of the instruction execution units.

25 The first conversion unit 133 performs "preprocessing" of the rearrangement of basic instructions, and the second conversion unit 134 performs "postprocessing" of the rearrangement of the basic instructions.

To improve the performance of the parallel processor in an actual circuit, the processes in the instruction fetch unit 62 and the instruction issue unit 88 are pipelined. Because of that, the difference in processing time between instruction fetch unit 62 and the instruction issue unit 88 should be as small as possible to optimize the pipeline effects. Therefore, the arrangement process is divided into the "preprocessing" and

"postprocessing", so that the difference in processing time between the instruction fetch unit 62 and the instruction issue unit 88 is small.

By the parallel processor 36 of this 5 example having the above structure, wires can be shortened as a whole, and the operation speed can be increased.

Additionally, the circuit size of the parallel processor 36 may be reduced by restricting 10 in advance the arrangement of basic instructions contained in each instruction word to be supplied to the instruction fetch unit 62, as in the foregoing examples.

(Example 4)

15 FIG. 31 shows the structure of a fourth example of the parallel processor in accordance with the fourth embodiment of the present invention. As shown in FIG. 31, the parallel processor 37 has the same structure as the parallel processor 25 shown in 20 FIG. 16, in that the instruction fetch unit 63 includes a conversion unit 135 and the instruction issue unit 89 includes a judgment unit 110.

The structure and operation of the conversion unit 135 are the same as the structure 25 and operation of the conversion unit 115 shown in FIGS. 10 and 11. On the other hand, the structure and operation of the judgment unit 110 are the same as the judgment unit 103 shown in FIG. 6.

By the parallel processor 37 of this 30 example having the above structure, the same effects as obtained by the parallel processor 25 of Example 4 of the second embodiment can be obtained. More specifically, the instruction issue unit 89 including the judgment unit 110 enables accurate and 35 efficient parallel processing of basic instructions, thereby increasing the reliability of the operation. The instruction fetch unit 63 including the

conversion unit 135 facilitates the issuance of basic instructions from the instruction issue unit 89 to the instruction execution units, thereby increasing the operation speed.

5 Additionally, the circuit size of the
parallel processor 37 may be reduced by restricting
in advance the arrangement of basic instructions
contained in each instruction word to be supplied to
the instruction fetch unit 63, as in the foregoing
10 examples.

(Example

FIG. 32 shows the structure of a fifth example of the parallel processor in accordance with the fourth embodiment of the present invention. As shown in FIG. 32, the parallel processor 38 has the same structure as the parallel processor 26 of Example 5 of the second embodiment shown in FIG. 18, in that the instruction issue unit 90 includes a conversion unit 136 and a judgment unit 111.

20 The structure and operation of the conversion unit 136 are the same as the structure and operation of the conversion unit 115 shown in FIGS. 10 and 11. On the other hand, the structure and operation of the judgment unit 111 are the same as the structure and operation of the judgment unit 103 shown in FIG. 6.

25

By the parallel processor of this example having the above structure, the same effects as obtained by the parallel processor 26 of Example 5 of the second embodiment can be obtained. More specifically, the instruction issue unit 90 including the judgment unit 111 enables accurate and efficient parallel processing of basic instructions, thereby increasing the reliability of the operation. The instruction issue unit 90 further including the conversion unit 136 facilitates the issuance of basic instruction to the instruction execution units.

thereby increasing the operation speed.

Additionally, the circuit size of the parallel processor 38 may be reduced by restricting in advance the arrangement of basic instructions 5 contained in each instruction word to be supplied to the instruction fetch unit 64, as in the foregoing examples.

(Example 6)

FIG. 33 shows the structure of a sixth 10 example of the parallel processor in accordance with the fourth embodiment of the present invention. As shown in FIG. 33, the parallel processor 39 has the same structure as the parallel processor 27 shown in FIG. 20.

15 The structures and operations of a first conversion unit 137 and a second conversion unit 138 are the same as the structures and operations of the first conversion unit 117 and the second conversion unit 118 shown in FIG. 14. On the other hand, the 20 structure and operation of the judgment unit 112 are the same as the structure and operation of the judgment unit 103 shown in FIG. 6.

By the parallel processor 39 of this example having the above structure, the same effects 25 as obtained by the parallel processor of Example 6 of the second embodiment can be obtained. More specifically, the instruction issue unit 91 including the judgment unit 112 enables accurate and efficient parallel processing of basic instructions, 30 thereby increasing the reliability of the operation. The instruction fetch unit 65 including the first conversion unit 137 and the instruction issue unit 91 further including the second conversion unit 138 facilitate the issuance of basic instructions from 35 the instruction issue unit 91 to the instruction execution units, thereby increasing the operation speed.

Additionally, the circuit size of the parallel processor 39 may be reduced by restricting in advance the arrangement of basic instructions contained in each instruction word to be supplied to 5 the instruction fetch unit 65, as in the foregoing examples.

[Fifth Embodiment]

As shown in FIGS. 34 to 39, parallel 10 processors 40 to 45 in accordance with a fifth embodiment of the present invention each comprise an instruction fetch unit 66-71 connected to the memory 12, an instruction issue unit 92-97 connected to the instruction fetch unit 66-71, instruction execution 15 units LU0, LU1, IU0, IU1, FU0, FU1, MU0, MU1, BU0, and BU1, and a register unit 102 connected to all the instruction execution units.

In the following, the parallel processor in accordance with the fifth embodiment of the 20 present invention will be described by way of examples in which the maximum basic instruction word length contained in each instruction word is 4. In FIGS. 34 to 39, the maximum basic instruction word length being 4 is indicated by four arrows extending 25 from the instruction issue unit 66-71 to the instruction issue unit 92-97.

It should be understood that the maximum basic instruction word length is not limited to 4 in this embodiment.

30 (Example 1)

FIG. 34 shows the structure of a first example of the parallel processor in accordance with the fifth embodiment of the present invention. As shown in FIG. 34, the parallel processor 40 35 comprises a conversion unit 139 in the instruction fetch unit 66. The structure and operation of the conversion unit 139 are the same as the structure

and operation of the conversion unit 115 of Example 1 of the second embodiment of the present invention. The conversion unit 139 rearranges basic instructions contained in each fetched instruction word, in accordance with the arrangement of the instruction execution units, and then supplies the rearranged basic instructions to the instruction issue unit 92.

By the parallel processor 40 having the above structure, the same effects as obtained by the parallel processor 22 of Example 1 of the second embodiment can be obtained. More specifically, the issuance of basic instruction from the instruction issue unit 92 to the instruction execution units can be facilitated, and the operation speed can be increased accordingly.

Additionally, the circuit size of the parallel processor 40 may be reduced by restricting in advance the arrangement of basic instructions contained in each instruction word to be supplied to the instruction fetch unit 66, as in the foregoing embodiments.

(Example 2)

FIG. 35 shows the structure of a second example of the parallel processor in accordance with the fifth embodiment of the present invention. As shown in FIG. 35, the parallel processor 41 has the same structure as the parallel processor 23 shown in FIG. 12, in that the instruction issue unit 93 includes a conversion unit 140. The structure and operation of the conversion unit 140 are the same as the structure and operation of the conversion unit 115 shown in FIGS. 10 and 11.

In the parallel processor 41 of this example, the instruction issue unit 93 rearranges basic instructions contained in each instruction word supplied from the instruction fetch unit 67.

and then supplies the rearranged basic instructions to the instruction execution units. Thus, wires can be shortened as a whole, and the operation speed can be increased.

5 Additionally, the circuit size of the parallel processor 41 may be reduced by restricting in advance the arrangement of basic instructions contained in each instruction word to be supplied to the instruction fetch unit 67, as in the foregoing
10 examples.

(Example 3)

FIG. 36 shows the structure of a third example of the parallel processor in accordance with the fifth embodiment of the present invention. As
15 shown in FIG. 36, the parallel processor 42 of this example has the same structure as the parallel processor 24 shown in FIG. 14. The instruction fetch unit 68 of the parallel processor 42 includes a first conversion unit 141 that rearranges basic
20 instructions contained in each fetched instruction word in accordance with the arrangement of the instruction execution units. The instruction issue unit 94 of the parallel processor 42 includes a second conversion unit 142 that further rearranges
25 basic instructions contained in each instruction word supplied from the instruction fetch unit 68 in accordance with the arrangement of the instruction execution units.

The first conversion unit 141 performs
30 "preprocessing" of the rearrangement of basic instructions, and the second conversion unit 142 performs "postprocessing" of the rearrangement of the basic instructions.

In order to improve the performance of the
35 parallel processor in an actual circuit, the processes in the instruction fetch unit 68 and the instruction issue unit 94 are pipelined. Because of

that, the difference in processing time between instruction fetch unit 68 and the instruction issue unit 94 should be as small as possible to optimize the pipeline effects. Therefore, the arrangement 5 process is divided into the "preprocessing" and "postprocessing", so that the difference in processing time between the instruction fetch unit 68 and the instruction issue unit 94 can be small.

By the parallel processor 42 of this 10 example having the above structure, wires can be shortened as a whole, and the operation speed can be increased.

Additionally, the circuit size of the parallel processor 42 may be reduced by restricting 15 in advance the arrangement of basic instructions contained in each instruction word to be supplied to the instruction fetch unit 68, as in the foregoing examples.

(Example 4)

20 FIG. 37 shows the structure of a fourth example of the parallel processor in accordance with the fifth embodiment of the present invention. As shown in FIG. 37, the parallel processor 43 has the same structure as the parallel processor 25 shown in 25 FIG. 16, in that the instruction fetch unit 69 includes a conversion unit 143 and the instruction issue unit 95 includes a judgment unit 113.

The structure and operation of the conversion unit 143 are the same as the structure 30 and operation of the conversion unit 115 shown in FIGS. 10 and 11. On the other hand, the structure and operation of the judgment unit 113 are the same as the structure and operation of the judgment unit 103 shown in FIG. 6.

35 By the parallel processor 43 of this example having the above structure, the same effects as obtained by the parallel processor 25 of Example

4 of the second embodiment can be obtained. More specifically, the instruction issue unit 95 including the judgment unit 113 enables accurate and efficient parallel processing of basic instructions, 5 thereby increasing the reliability of the operation. The instruction fetch unit 69 including the conversion unit 143 facilitates the issuance of basic instructions from the instruction issue unit 95 to the instruction execution units, thereby 10 increasing the operation speed.

Additionally, the circuit size of the parallel processor 43 may be reduced by restricting in advance the arrangement of basic instructions contained in each instruction word to be supplied to 15 the instruction fetch unit 69, as in the foregoing examples.

(Example 5)

FIG. 38 shows the structure of a fifth example of the parallel processor in accordance with 20 the fifth embodiment of the present invention. As shown in FIG. 38, the parallel processor 44 of this example has the same structure as the parallel processor 26 of Example 5 of the second embodiment shown in FIG. 18, in that the instruction issue unit 25 96 includes a conversion unit 144 and a judgment unit 114.

The structure and operation of the conversion unit 144 are the same as the structure and operation of the conversion unit 115 shown in 30 FIGS. 10 and 11. On the other hand, the structure and operation of the judgment unit 114 are the same as the structure and operation of the judgment unit 103 shown in FIG. 6.

By the parallel processor 44 of this 35 example having the above structure, the same effects as obtained by the parallel processor 26 of Example 5 of the second embodiment can be obtained. More

specifically, the instruction issue unit 96 including the judgment unit 114 enables accurate and efficient parallel processing of basic instructions, thereby increasing the reliability of the operation.

5 The instruction issue unit 96 further including the conversion unit 144 facilitates the issuance of basic instructions to the instruction execution units, thereby increasing the operation speed.

10 Additionally, the circuit size of the parallel processor 44 may be reduced by restricting in advance the arrangement of basic instructions contained in each instruction word to be supplied to the instruction fetch unit 70, as in the foregoing examples.

15 (Example 6)

FIG. 39 shows the structure of a sixth example of the parallel processor in accordance with the fifth embodiment of the present invention. As shown in FIG. 39, the parallel processor 45 of this 20 example has the same structure as the parallel processor 27 shown in FIG. 20. The instruction fetch unit 71 includes a first conversion unit 145, and the instruction issue unit 97 includes a second conversion unit 146 and a judgment unit 219.

25 The structures and operations of the first conversion unit 145 and the second conversion unit 146 are the same as the structures and operations of the first conversion unit 117 and the second conversion unit 118 shown in FIG. 14. On the other 30 hand, the structure and operation of the judgment unit 219 are the same as the structure and operation of the judgment unit 103 shown in FIG. 6.

35 By the parallel processor 45 of this example having the above structure, the same effects as obtained by the parallel processor 27 of Example 6 of the second embodiment can be obtained. More specifically, the instruction issue unit 97

including the judgment unit 219 enables accurate and efficient parallel processing of basic instructions, thereby increasing the reliability of the operation. The instruction fetch unit 71 including the first 5 conversion unit 145 and the instruction issue unit 97 including the second conversion unit 146 facilitate the issuance of basic instructions from the instruction issue unit 97 to the instruction execution units, thereby increasing the operation 10 speed.

Additionally, the circuit size of the parallel processor 45 may be reduced by restricting in advance the arrangement of basic instructions contained in each instruction word to be supplied to 15 the instruction fetch unit 71, as in the foregoing examples.

The present invention is not limited to the specifically disclosed embodiments, but variations and modifications may be made without 20 departing from the scope of the present invention.

The present application is based on Japanese priority application No. 11-281957, filed on October 1, 1999, the entire contents of which are hereby incorporated by reference.

WHAT IS CLAIMED IS:

5

1. A parallel processor that performs parallel processing of one or more basic instructions contained in each of instruction words delimited by instruction delimiting information,
10 said parallel processor comprising:

a plurality of instruction execution units that perform processes corresponding to supplied basic instructions in parallel;

15 an instruction fetch unit that fetches the instruction words one by one in accordance with the instruction delimiting information; and

20 an instruction issue unit that selectively issues each of the basic instructions supplied from the instruction fetch unit to one of the instruction execution units to execute an issued basic instruction.

25

2. The parallel processor as claimed in claim 1, wherein the plurality of instruction execution units all have the same structure.

30

3. The parallel processor as claimed in claim 1, wherein:

35 at least two of the instruction execution units have different structures from each other; and the instruction fetch unit rearranges the

09554523 090 001

basic instructions contained in each of the fetched instruction words, in accordance with arrangement of the plurality of instruction execution units, and then supplies the rearranged basic instructions to the instruction issue unit.

10 4. The parallel processor as claimed in
claim 1, wherein:

at least two of the instruction execution units have different structures from each other; and the instruction issue unit rearranges the 15 basic instructions contained in each of the instruction words supplied from the instruction fetch unit, in accordance with arrangement of the plurality of instruction execution units, and then supplies the rearranged basic instructions to the 20 instruction execution units.

25 5. The parallel processor as claimed in
claim 1, wherein:

at least two of the instruction execution units have different structures from each other; the instruction fetch unit rearranges the basic instructions contained in each of the fetched instruction words, in accordance with arrangement of the instruction execution units, and then supplies the rearranged basic instructions to the instruction issue unit; and

35 the instruction issue unit further rearranges the basic instructions contained in each of the instruction word supplied from the

instruction fetch unit, in accordance with the arrangement of the instruction execution units, and then supplies the rearranged basic instructions to the instruction execution units.

5

6. The parallel processor as claimed in
10 claim 3, wherein:

at least two of the instruction execution units have different structures from each other; and
the instruction fetch unit fetches an instruction word that contains basic instruction
15 arranged in advance in accordance with the arrangement of the instruction execution units.

20

7. The parallel processor as claimed in
claim 1, wherein, depending on the type of a basic instruction being currently executed by one of the instruction execution units, the instruction issue
25 unit issues a next basic instruction before the execution of a basic instruction being currently executed is completed.

30

8. The parallel processor as claimed in
claim 7, wherein, if a supplied basic instruction does not have data dependency or control dependency,
35 or does not share resources with a basic instruction being currently executed by one of the instruction execution units, the instruction issue unit issues

the supplied basic instruction before the execution of the basic instruction being currently executed is completed.

ABSTRACT OF THE DISCLOSURE

A parallel processor that performs efficient parallel processing is provided. The parallel processor, which performs parallel processing of one or more basic instructions contained in each of instruction words delimited by instruction delimiting information, includes: a plurality of instruction execution units that perform processes corresponding to supplied basic instructions in parallel; an instruction fetch unit that fetches the instruction words one by one in accordance with the instruction delimiting information; and an instruction issue unit that issues each of the basic instructions contained in each of the instruction words fetched by the instruction fetch unit to a corresponding one of the instruction execution units.

FIG. 1 PRIOR ART

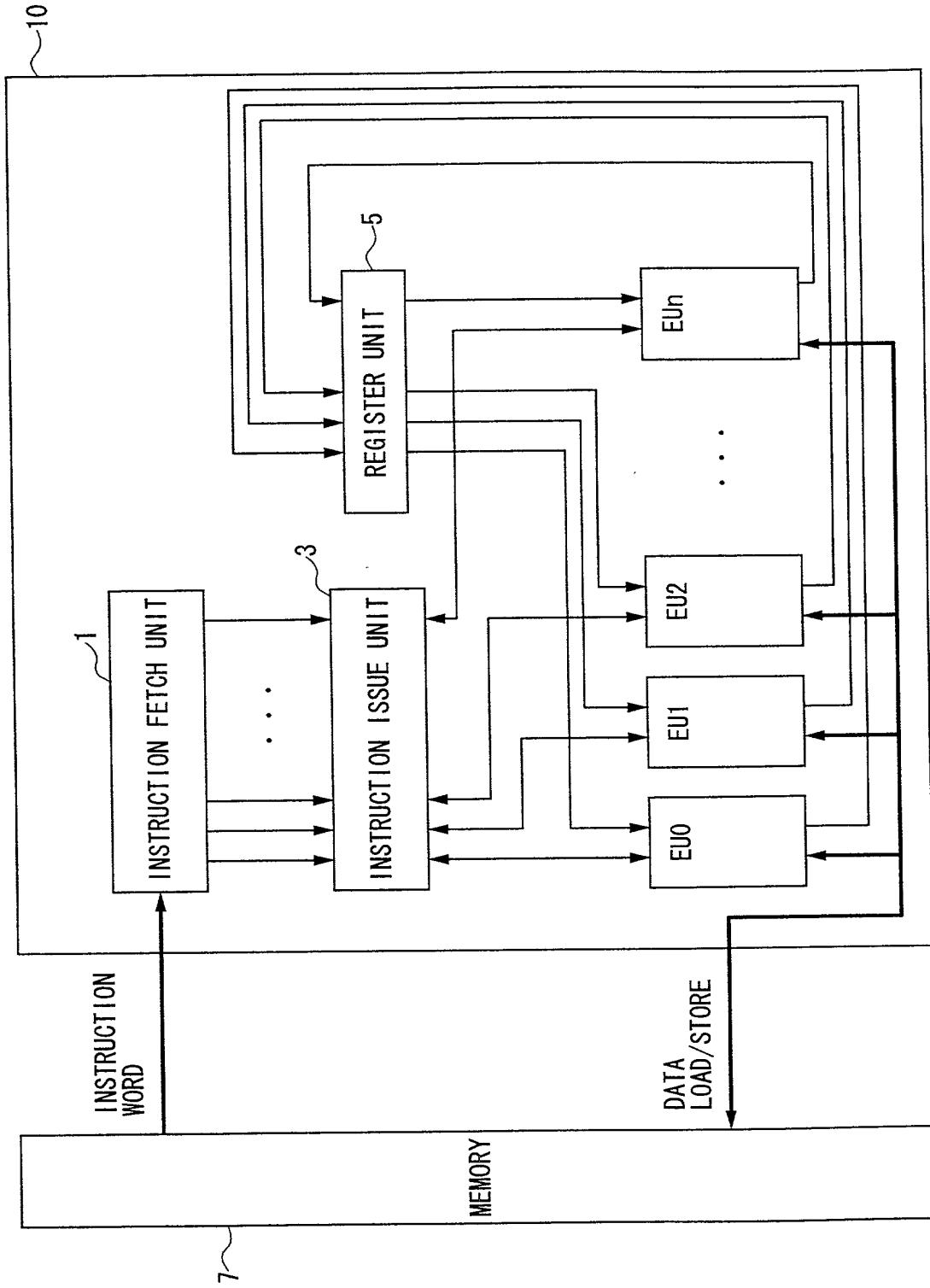


FIG.2

NOP	NOP	NOP	NOP
E1	NOP	NOP	NOP
NOP	E1	NOP	NOP
NOP	NOP	E1	NOP
NOP	NOP	NOP	E1
E1	E1	NOP	NOP
E1	NOP	E1	NOP
E1	NOP	NOP	E1
NOP	E1	E1	NOP
NOP	E1	NOP	E1
NOP	NOP	E1	E1
E1	E1	E1	NOP
E1	E1	NOP	E1
E1	NOP	E1	E1
NOP	E1	E1	E1
E1	E1	E1	E1

FIG.3

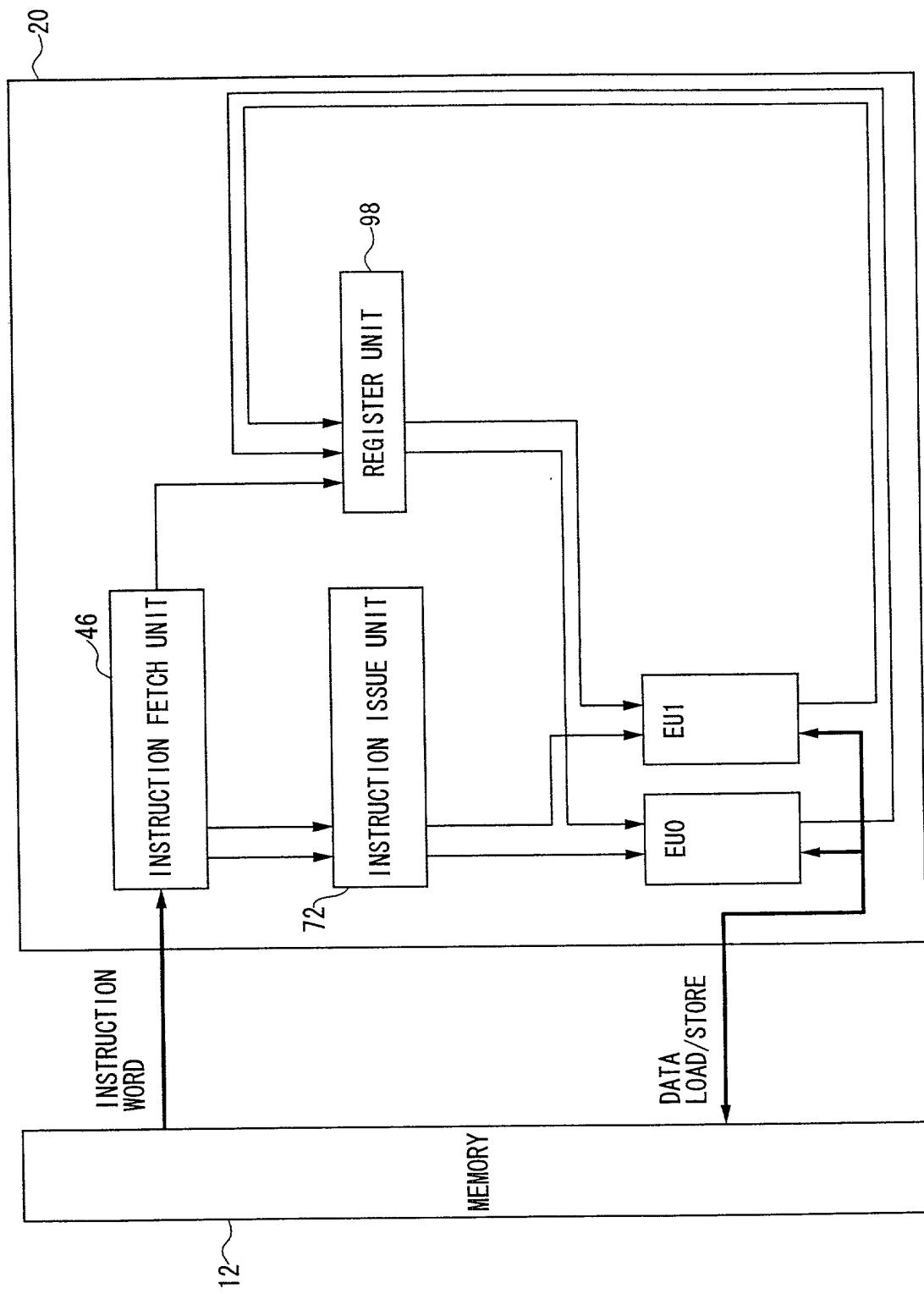


FIG.4

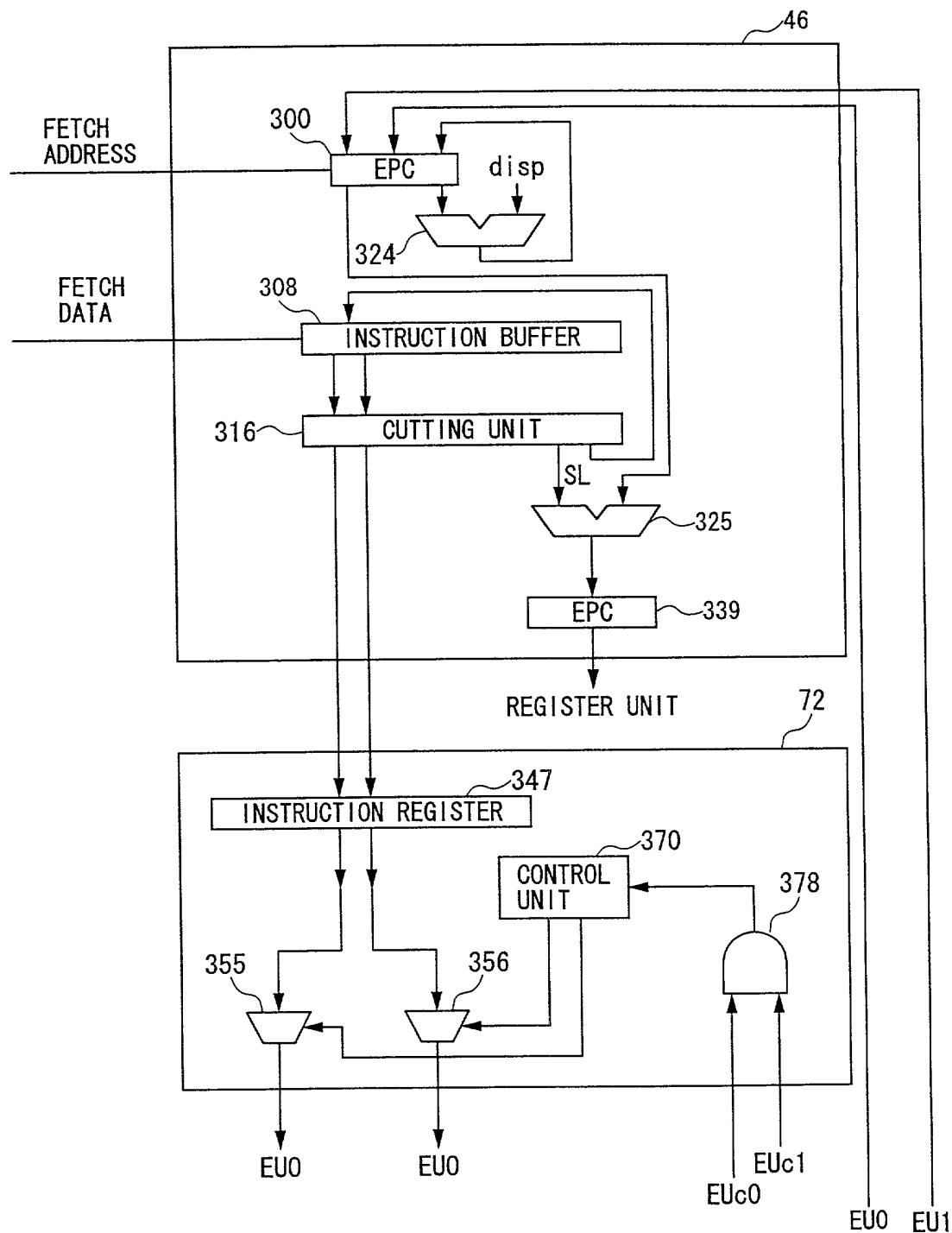


FIG. 5

0	EI	1	EI
1	EI		

FIG.6

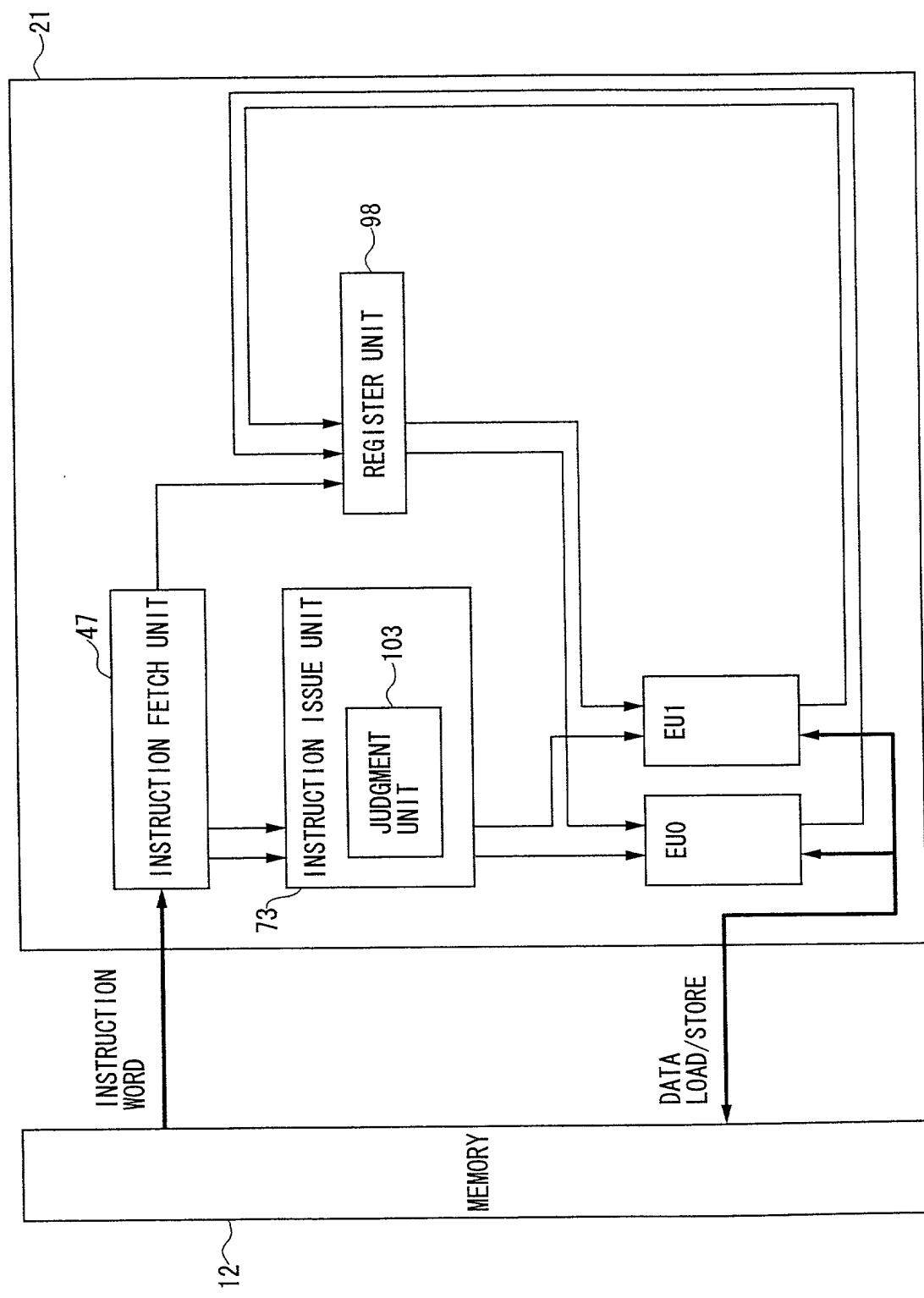


FIG. 7

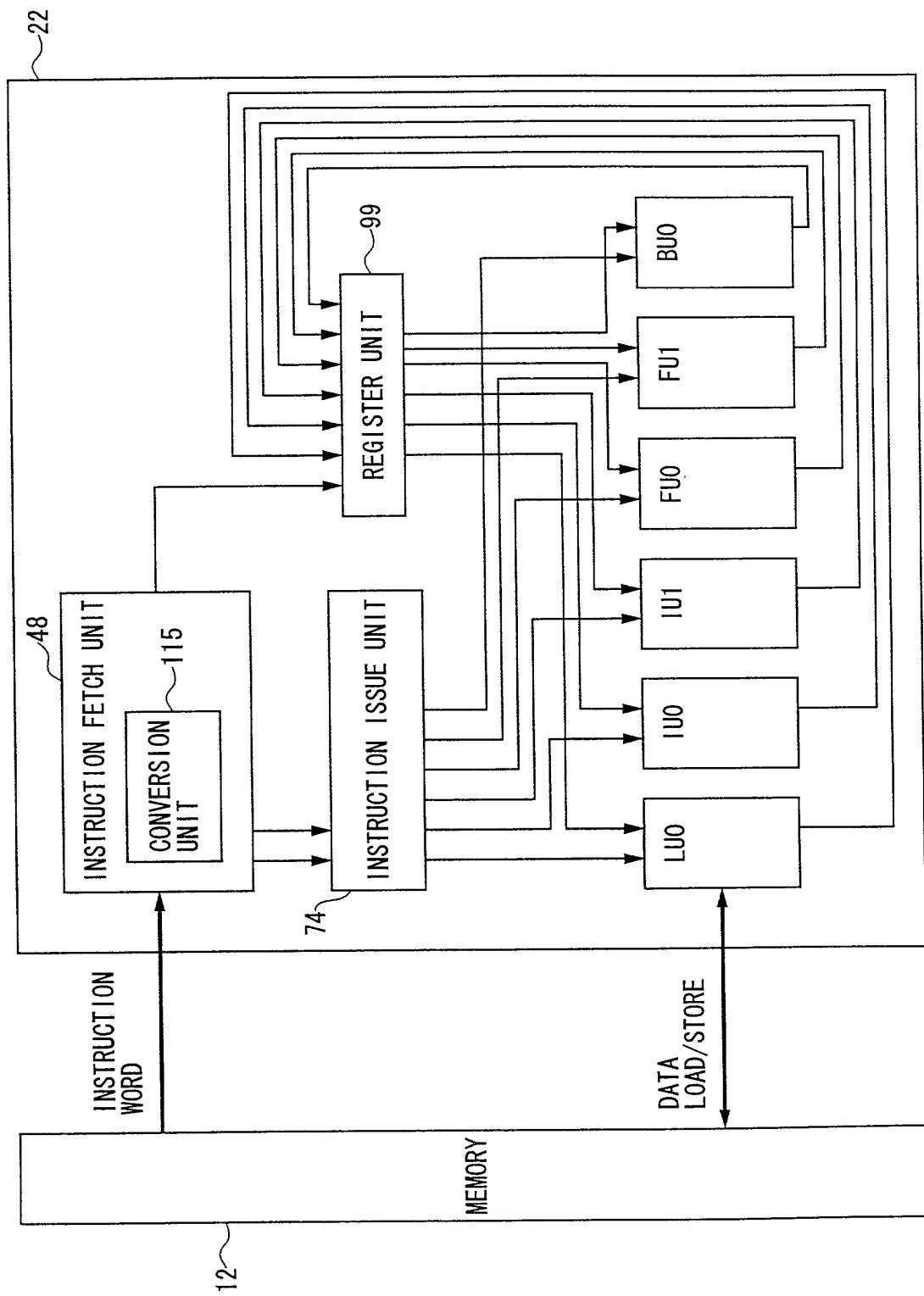


FIG.8

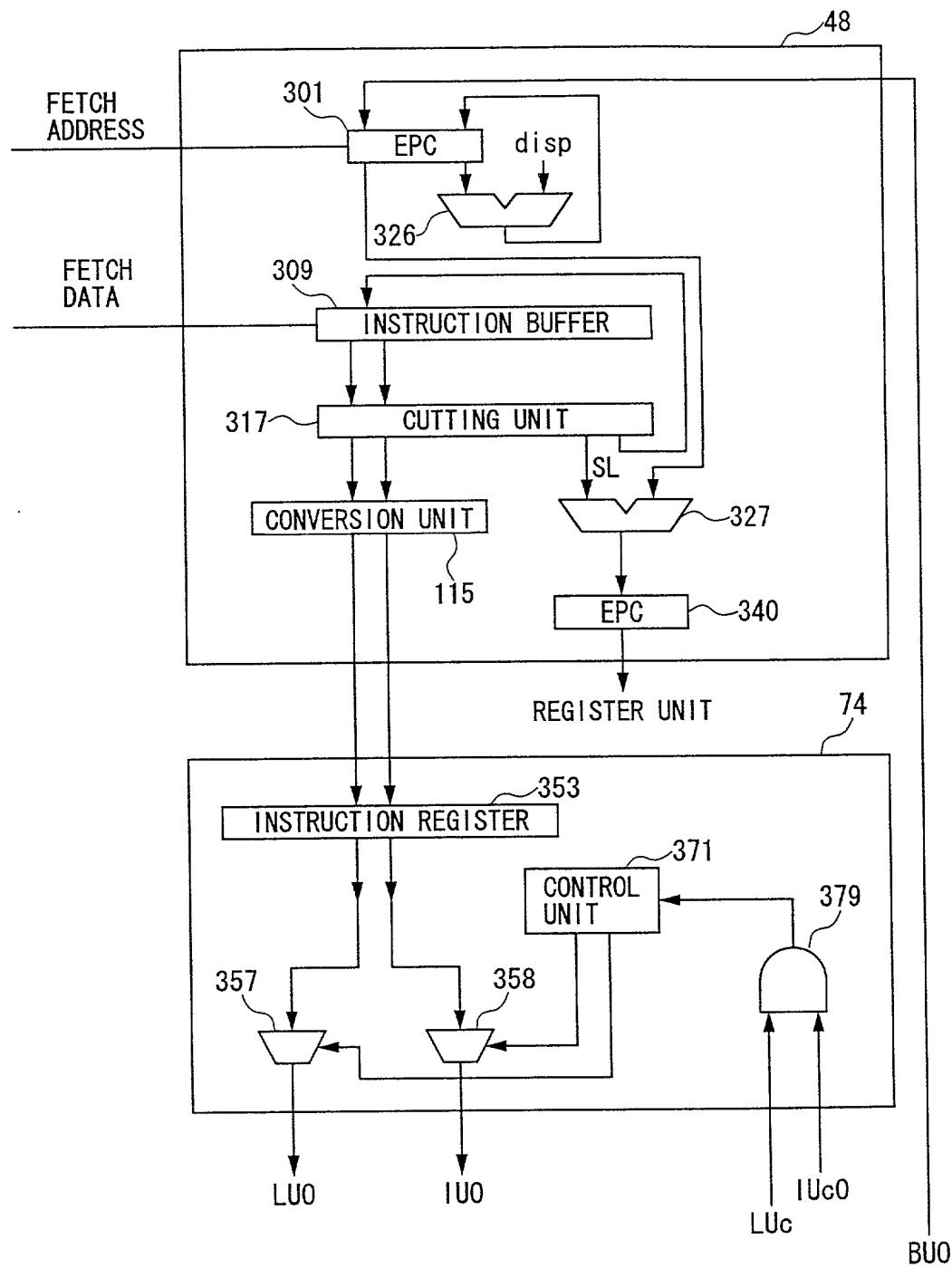


FIG. 9

13

FORMAT OF INSTRUCTION WORDS				LU0	IU0	IU1	FU0	FU1	BU0						
				V	LI	V	II	V	II	V	FI	V	FI	V	BI
0	BI	1	FI	0	-	0	-	0	-	1	FI	0	-	1	BI
0	BI	1	II	0	-	1	II	0	-	0	-	0	-	1	BI
0	BI	1	LI	1	LI	0	-	0	-	0	-	0	-	1	BI
0	FI	1	BI	0	-	0	-	0	-	1	FI	0	-	1	BI
0	FI	1	FI	0	-	0	-	0	-	1	FI	1	FI	0	-
0	FI	1	II	0	-	1	II	0	-	1	FI	0	-	0	-
0	FI	1	LI	1	LI	0	-	0	-	1	FI	0	-	0	-
0	II	1	BI	0	-	1	II	0	-	0	-	0	-	1	BI
0	II	1	FI	0	-	1	II	0	-	1	FI	0	-	0	-
0	II	1	II	0	-	1	II	1	II	0	-	0	-	0	-
0	II	1	LI	1	LI	1	II	0	-	0	-	0	-	0	-
0	LI	1	BI	1	LI	0	-	0	-	0	-	0	-	1	BI
0	LI	1	FI	1	LI	0	-	0	-	1	FI	0	-	0	-
0	LI	1	II	1	LI	1	II	0	-	0	-	0	-	0	-
1	BI			0	-	0	-	0	-	0	-	0	-	1	BI
1	FI			0	-	0	-	0	-	1	FI	0	-	0	-
1	II			0	-	1	II	0	-	0	-	0	-	0	-
1	LI			1	LI	0	-	0	-	0	-	0	-	0	-

15

17

FIG.10

INSTRUCTION WORD

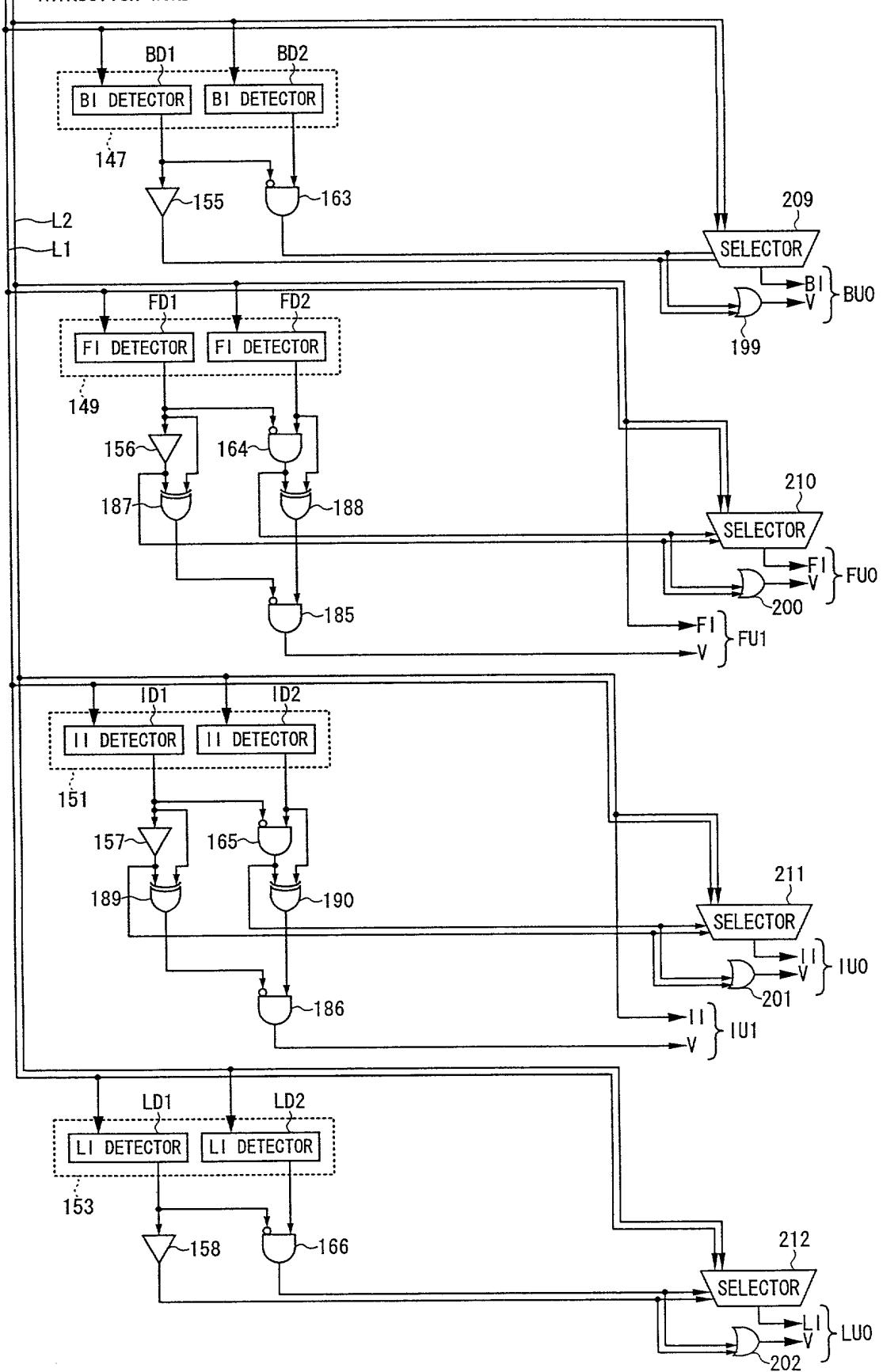


FIG. 11

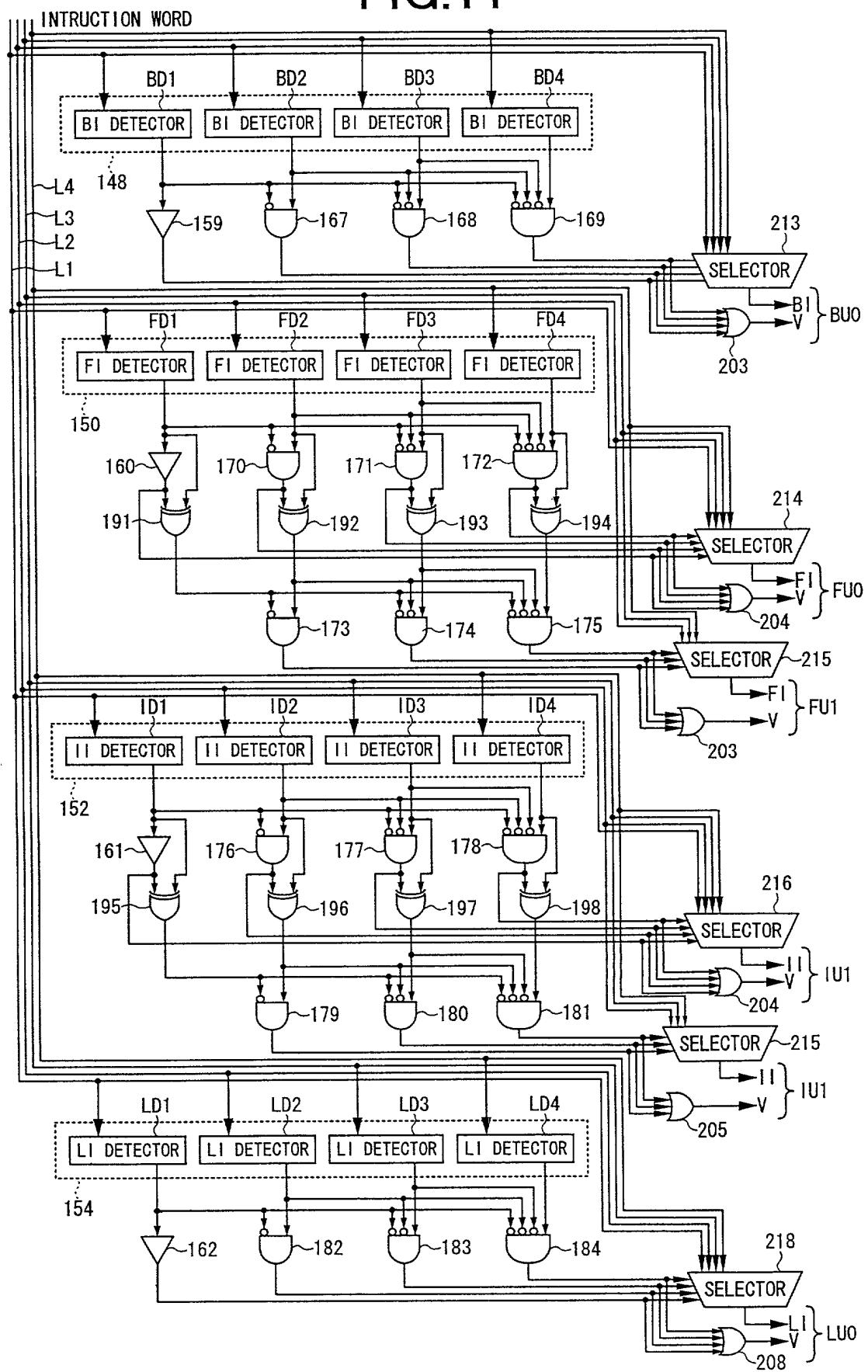


FIG. 12

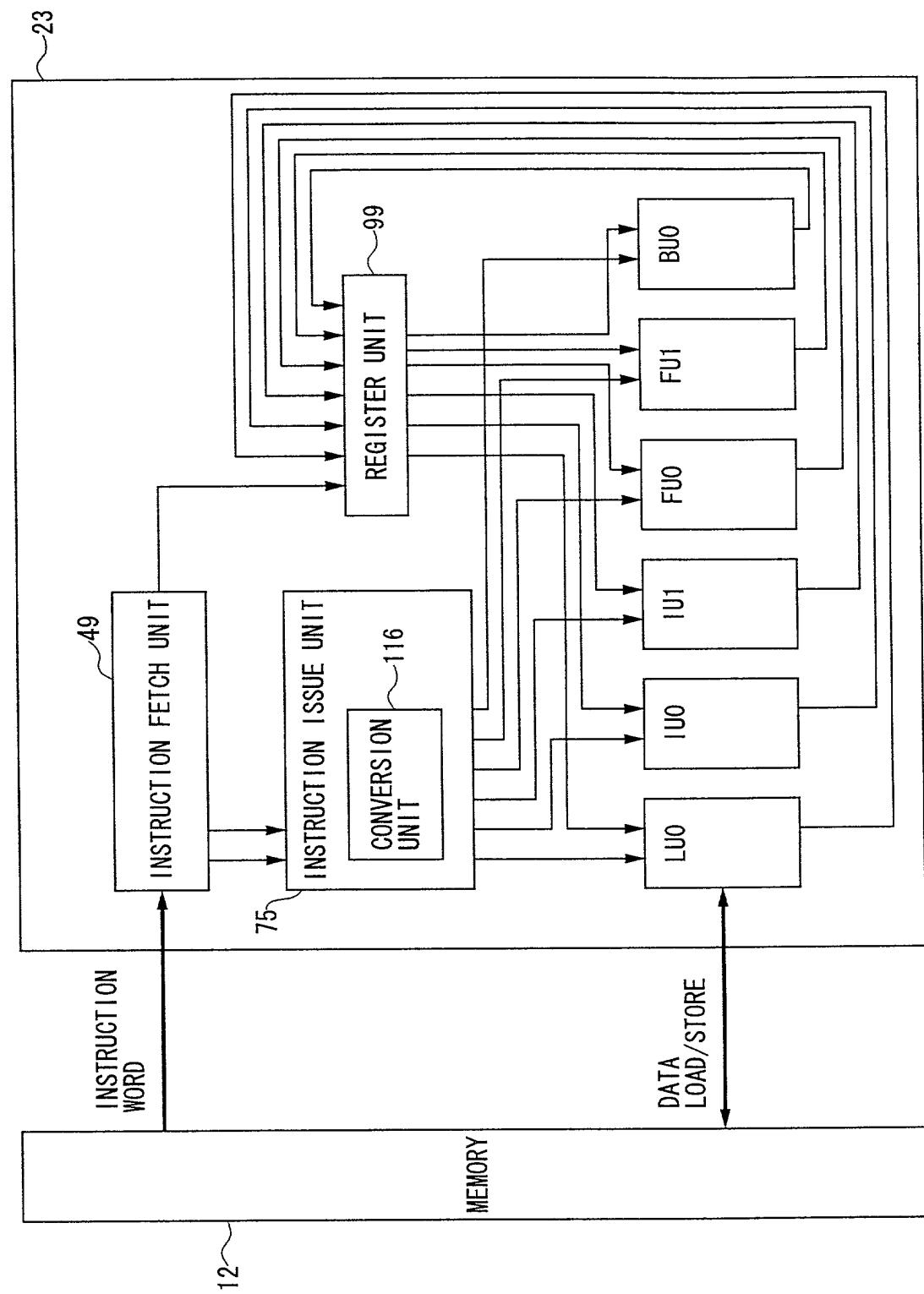


FIG.13

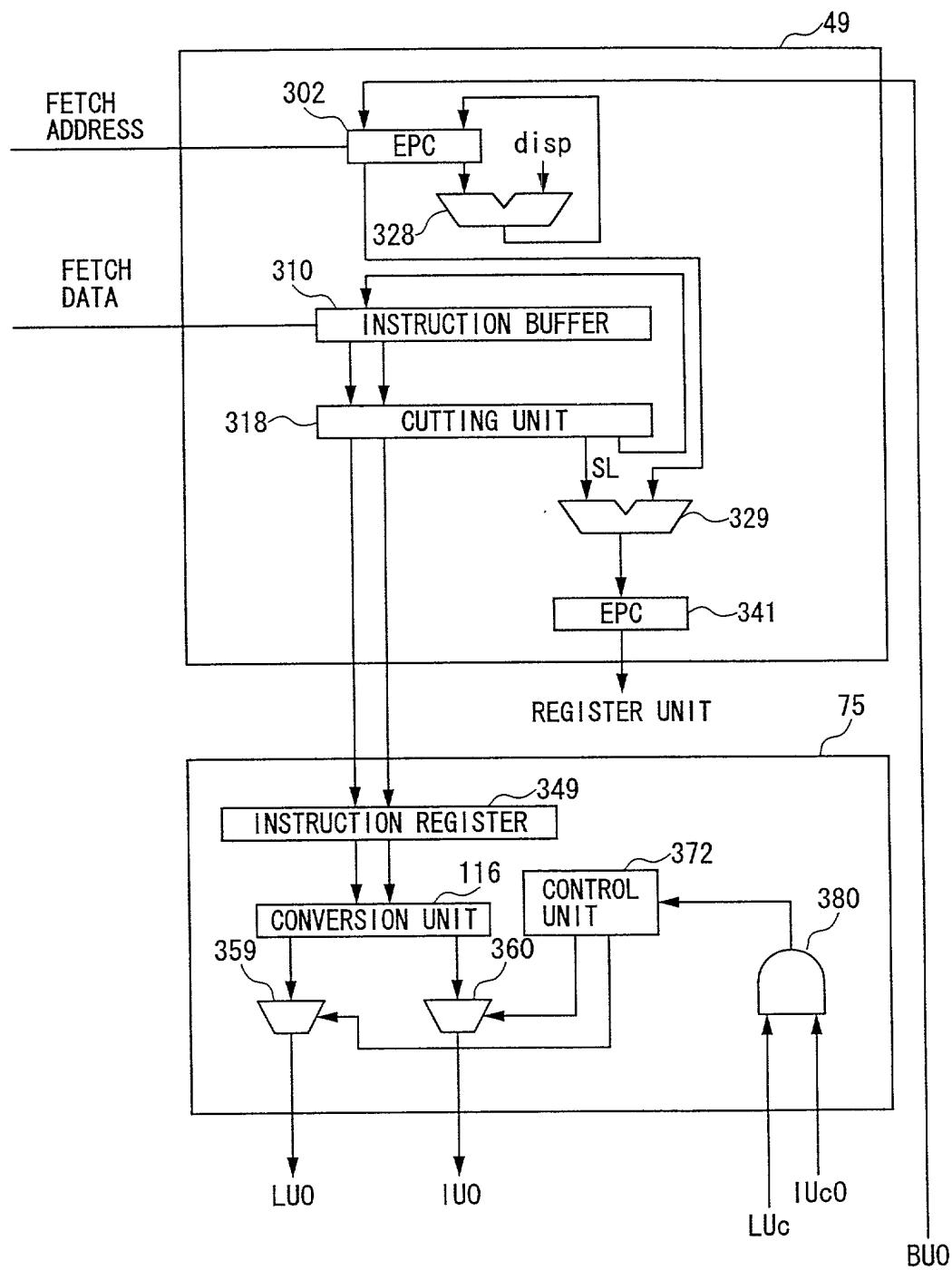


FIG. 14

24

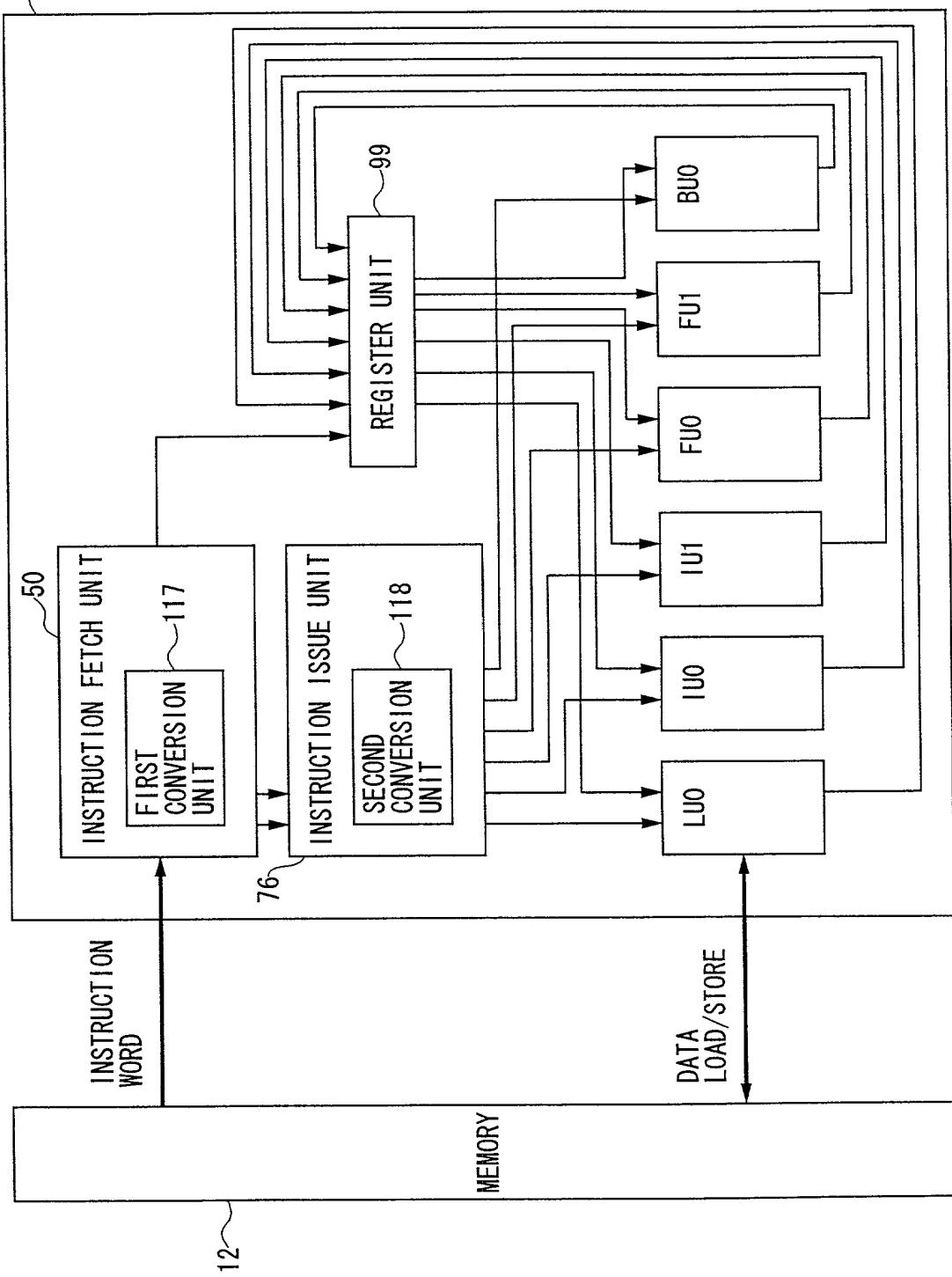


FIG.15

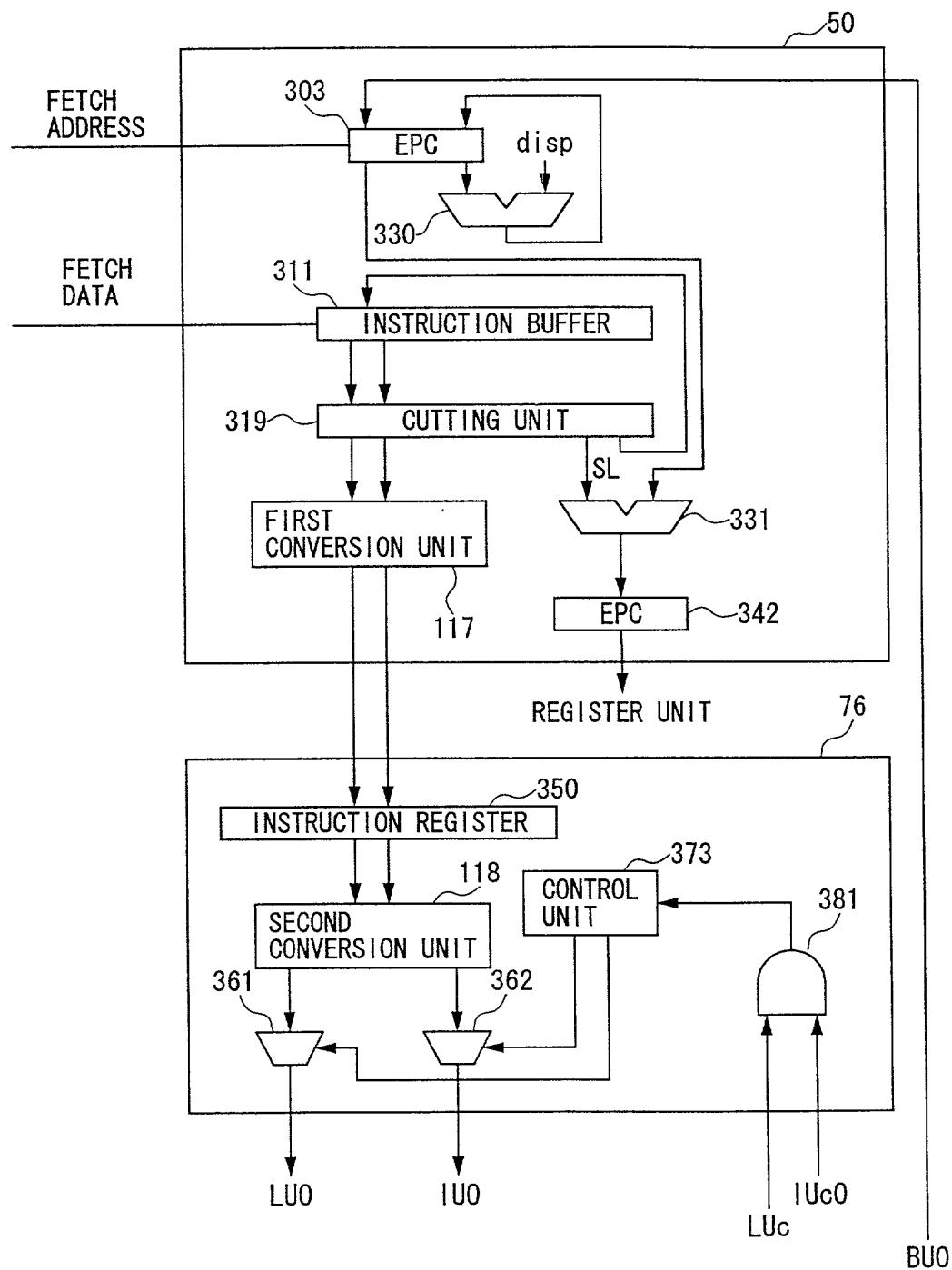


FIG. 16

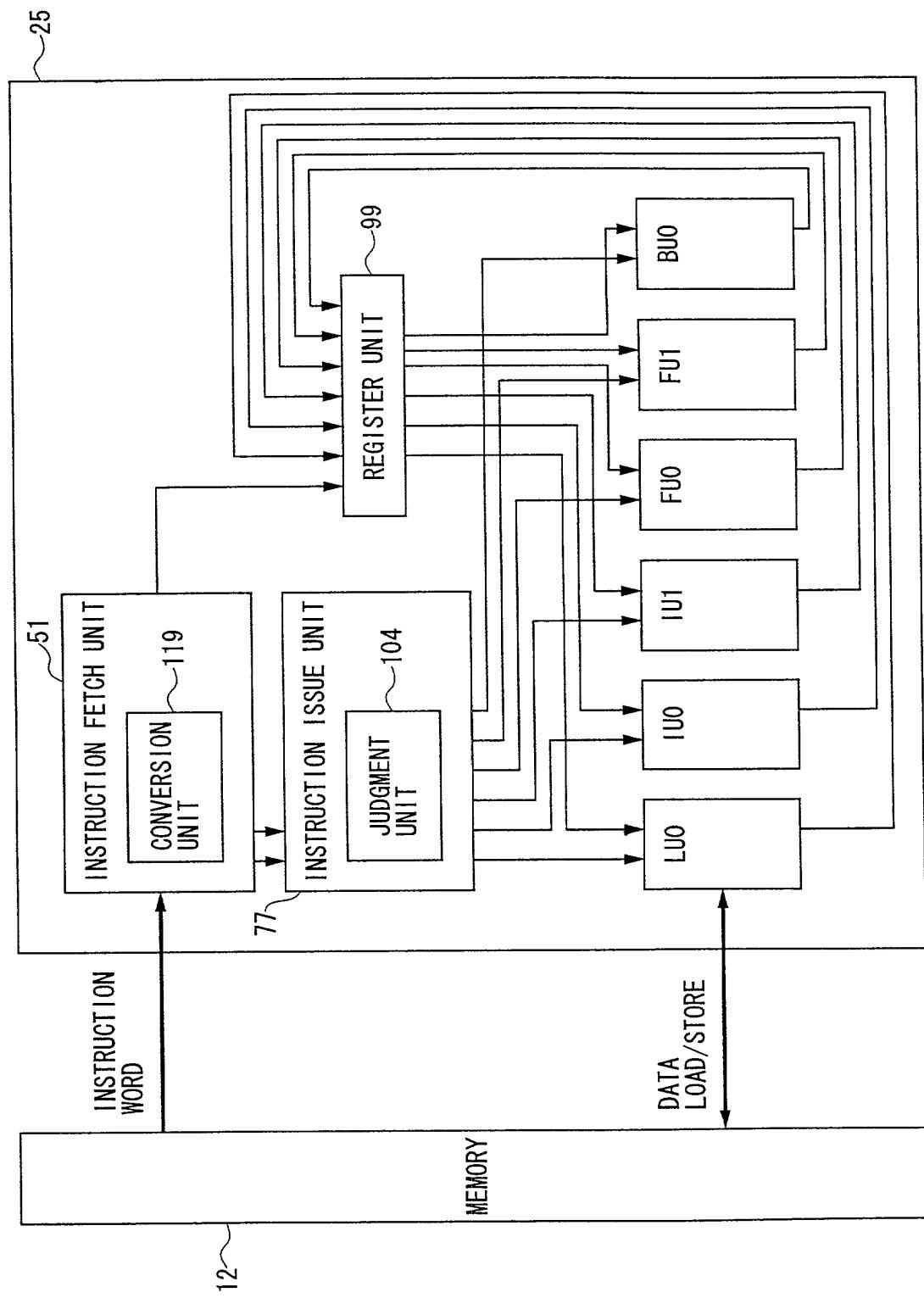


FIG.17

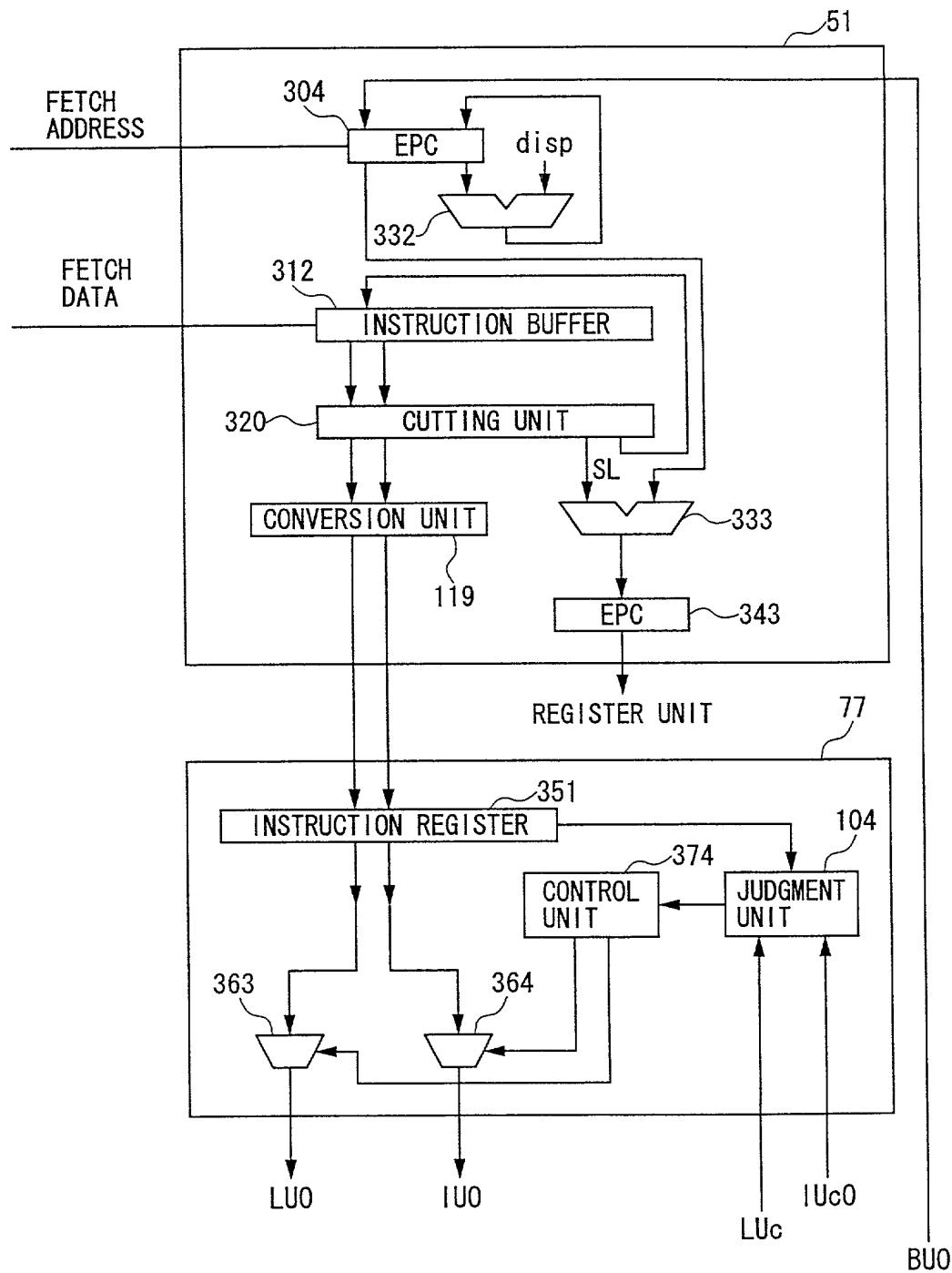


FIG. 18

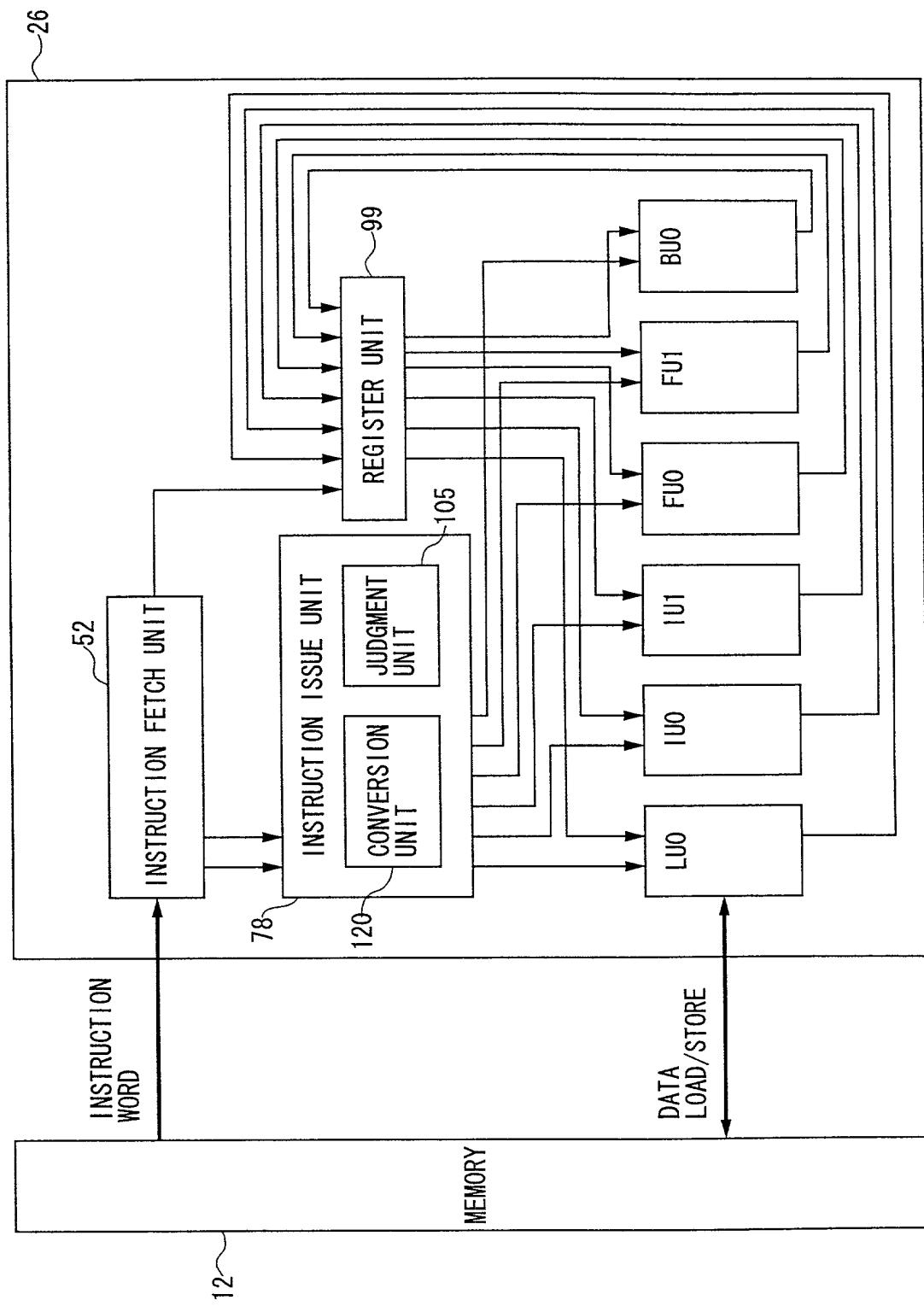


FIG.19

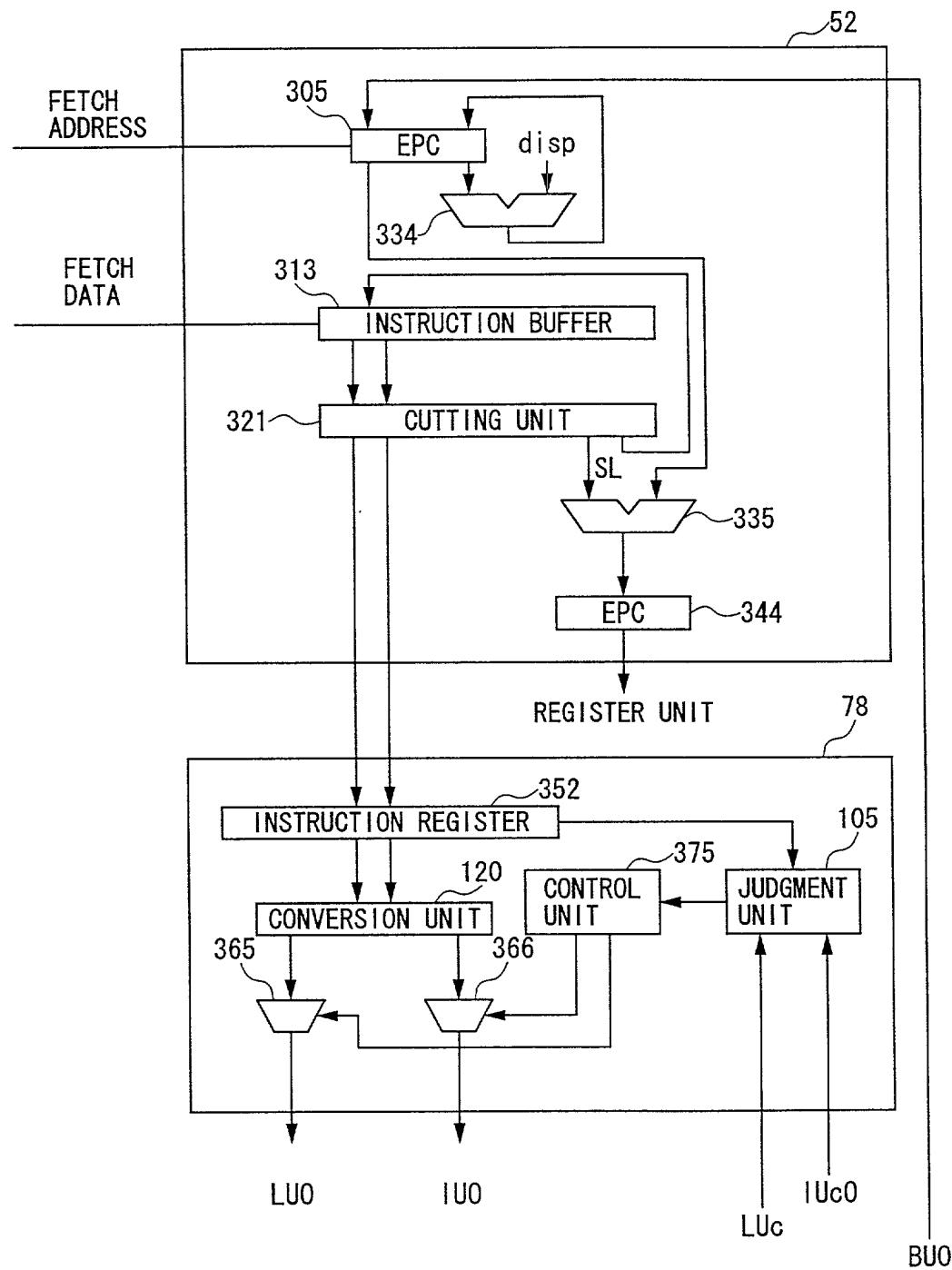


FIG.20

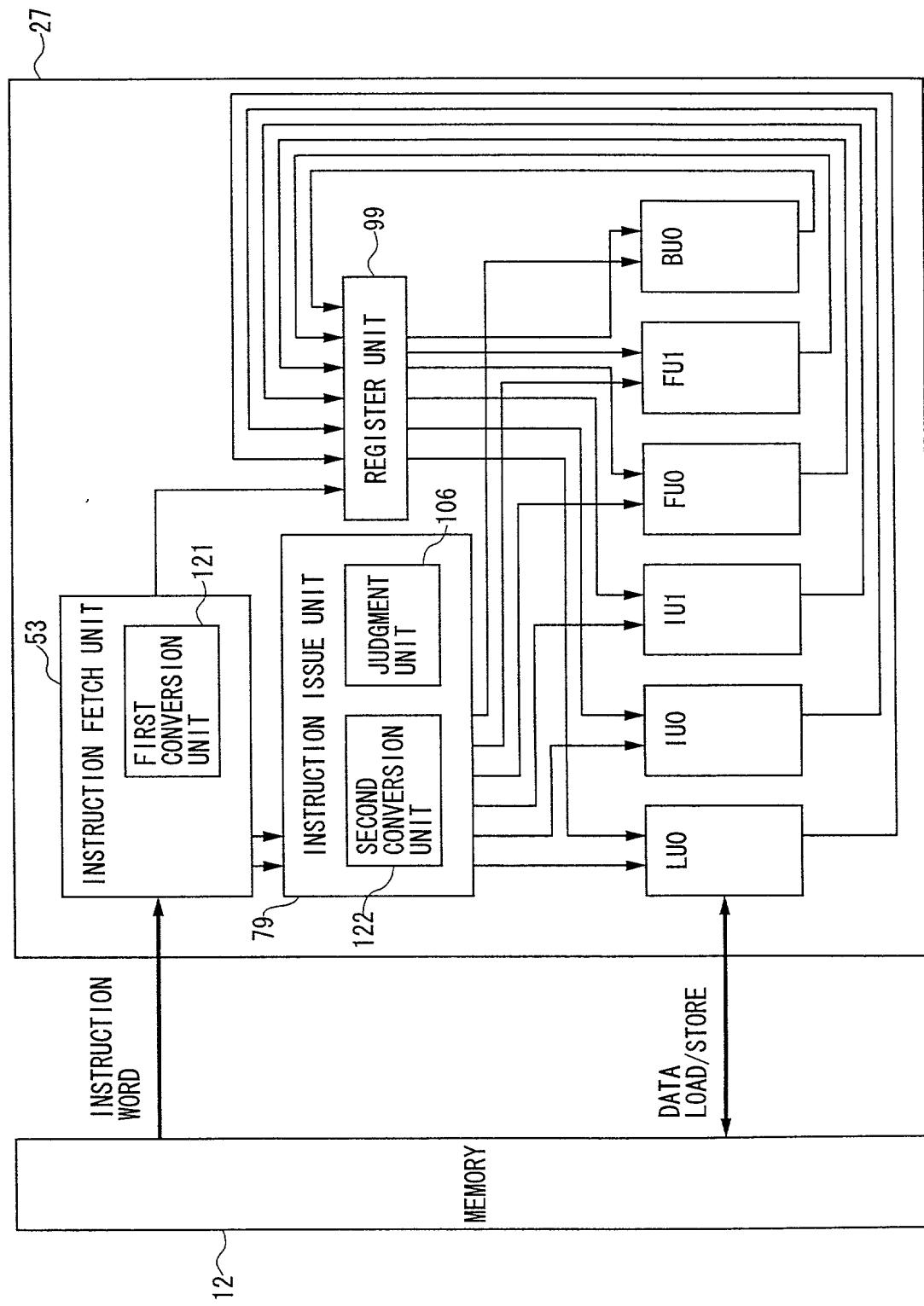


FIG.21

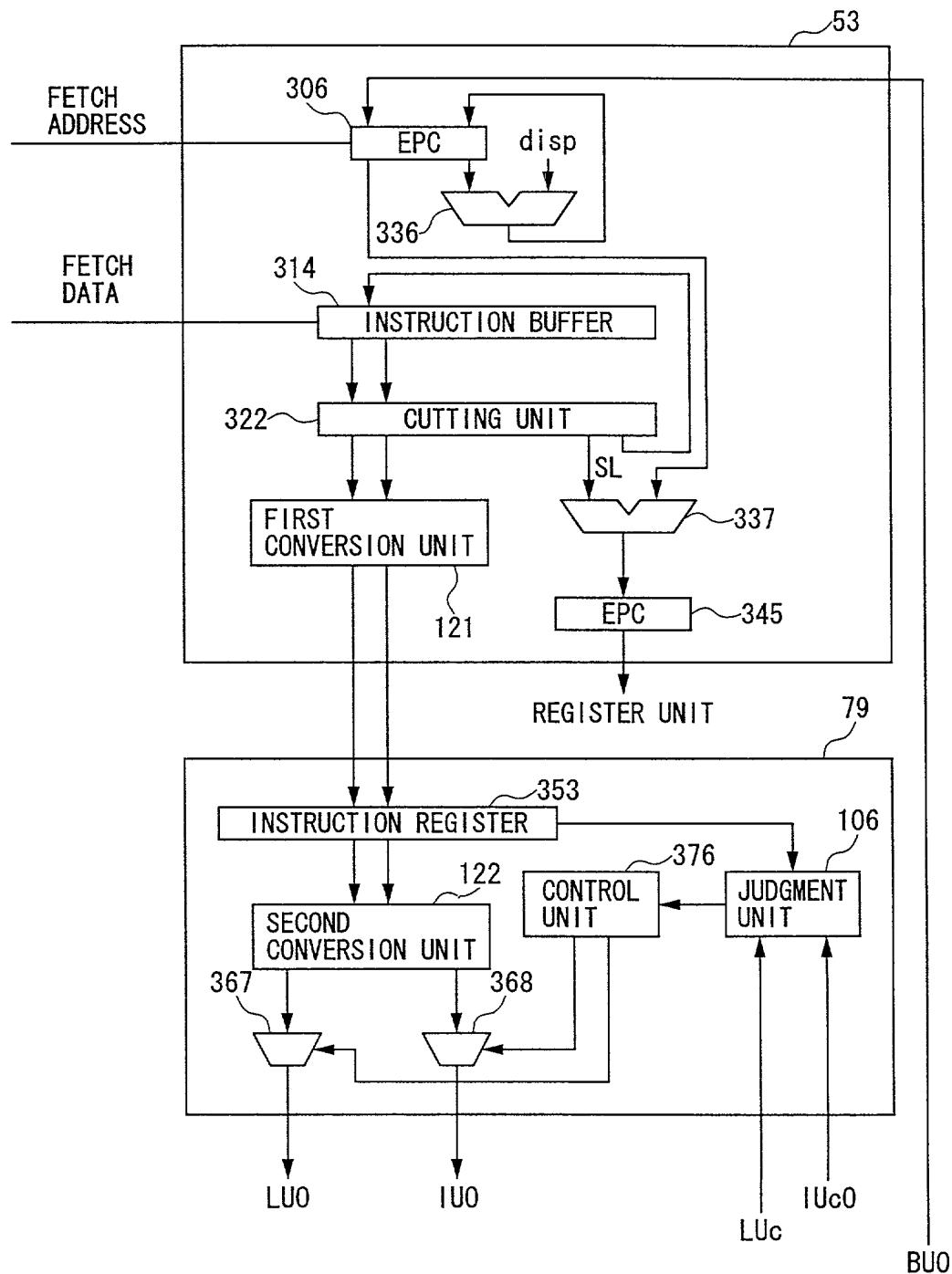


FIG.22

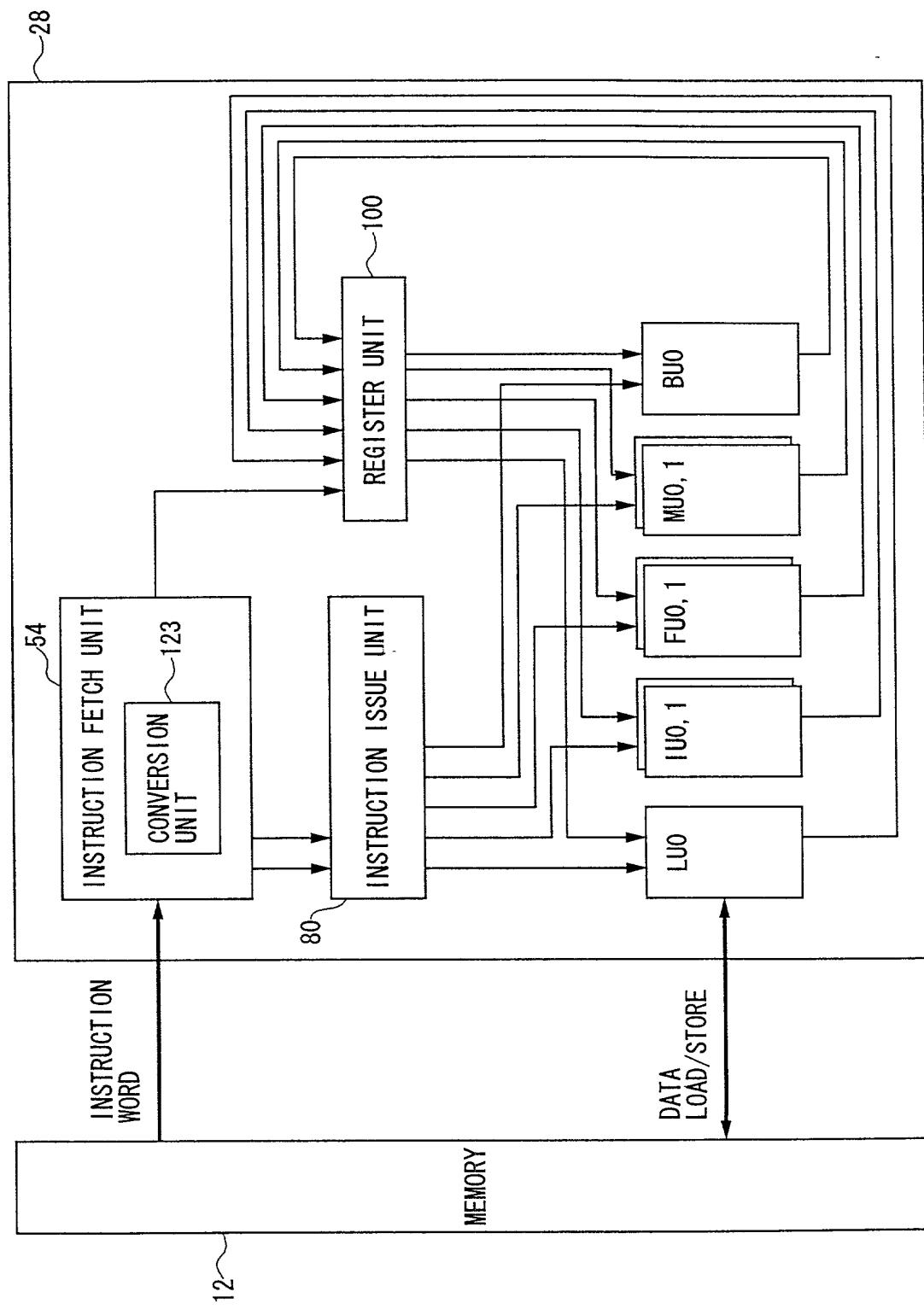


FIG.23

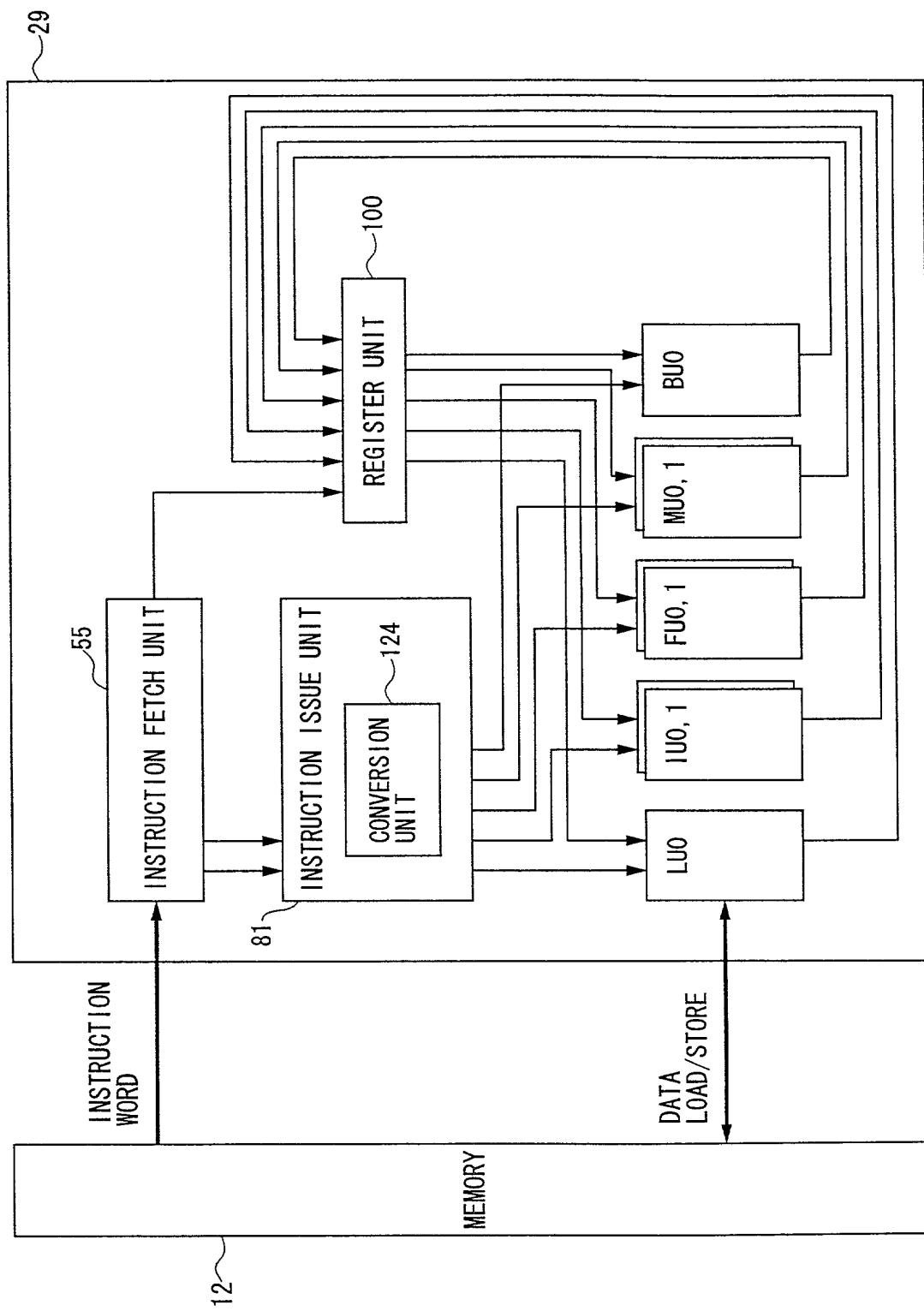


FIG.24

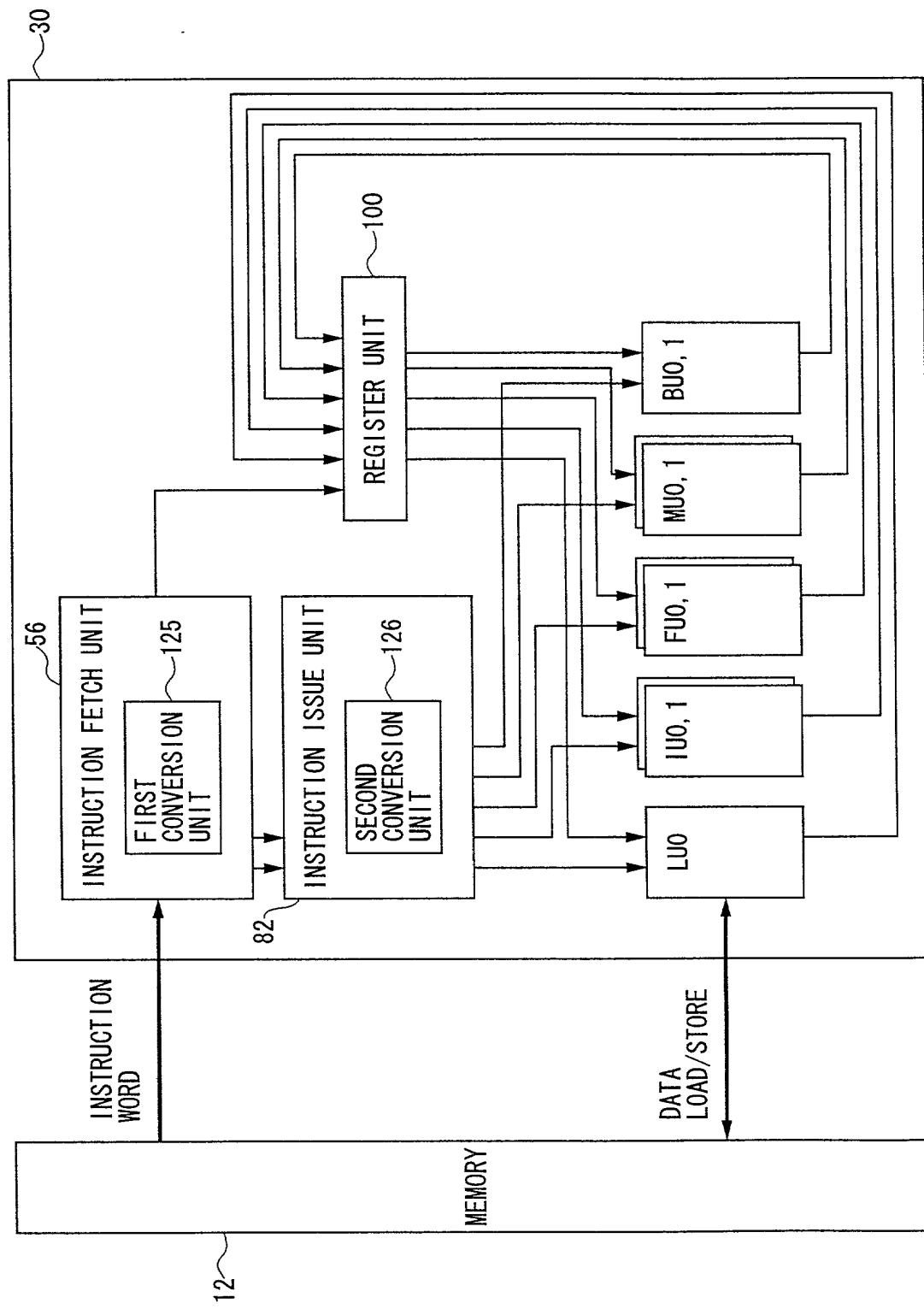


FIG.25

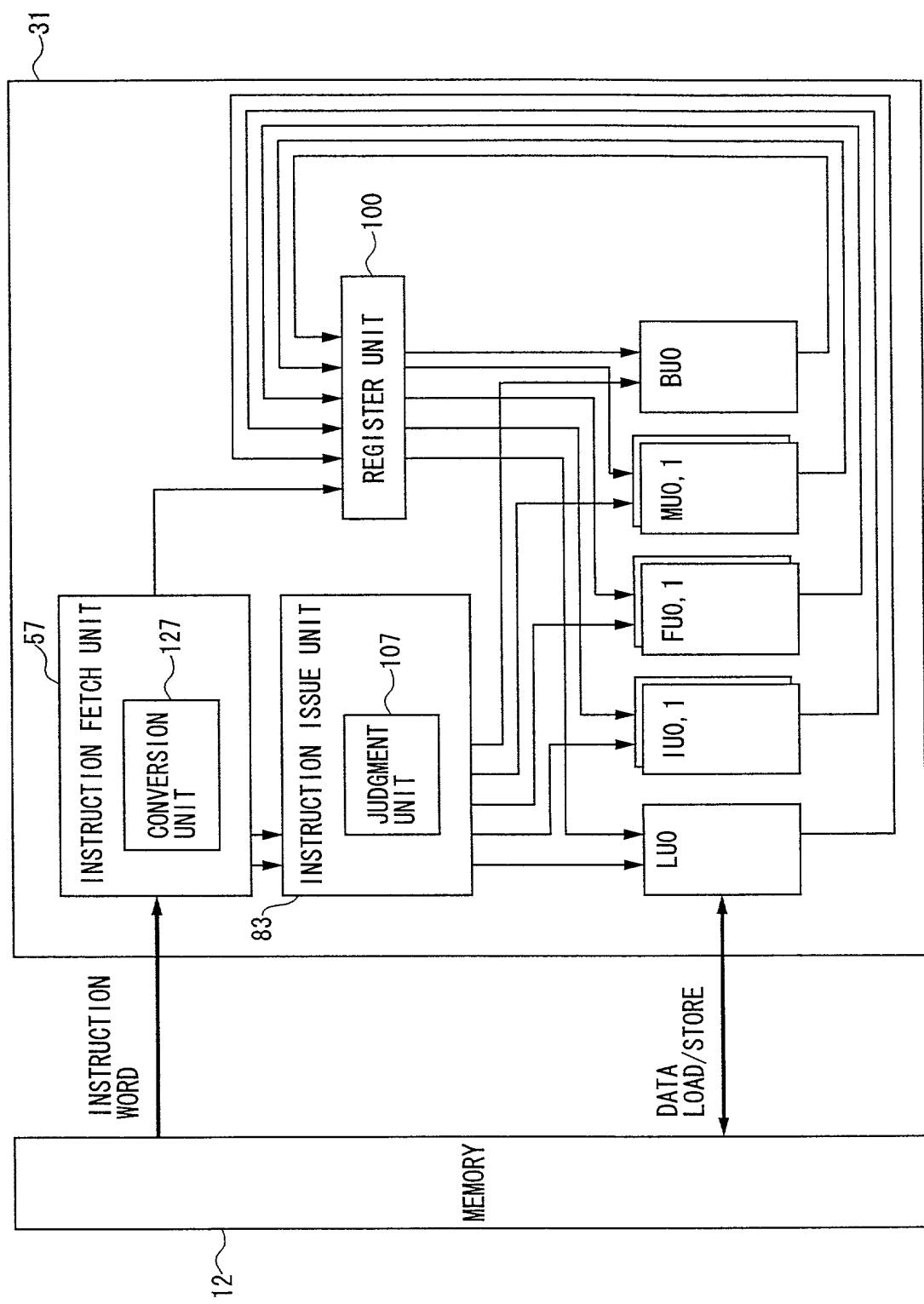


FIG.26

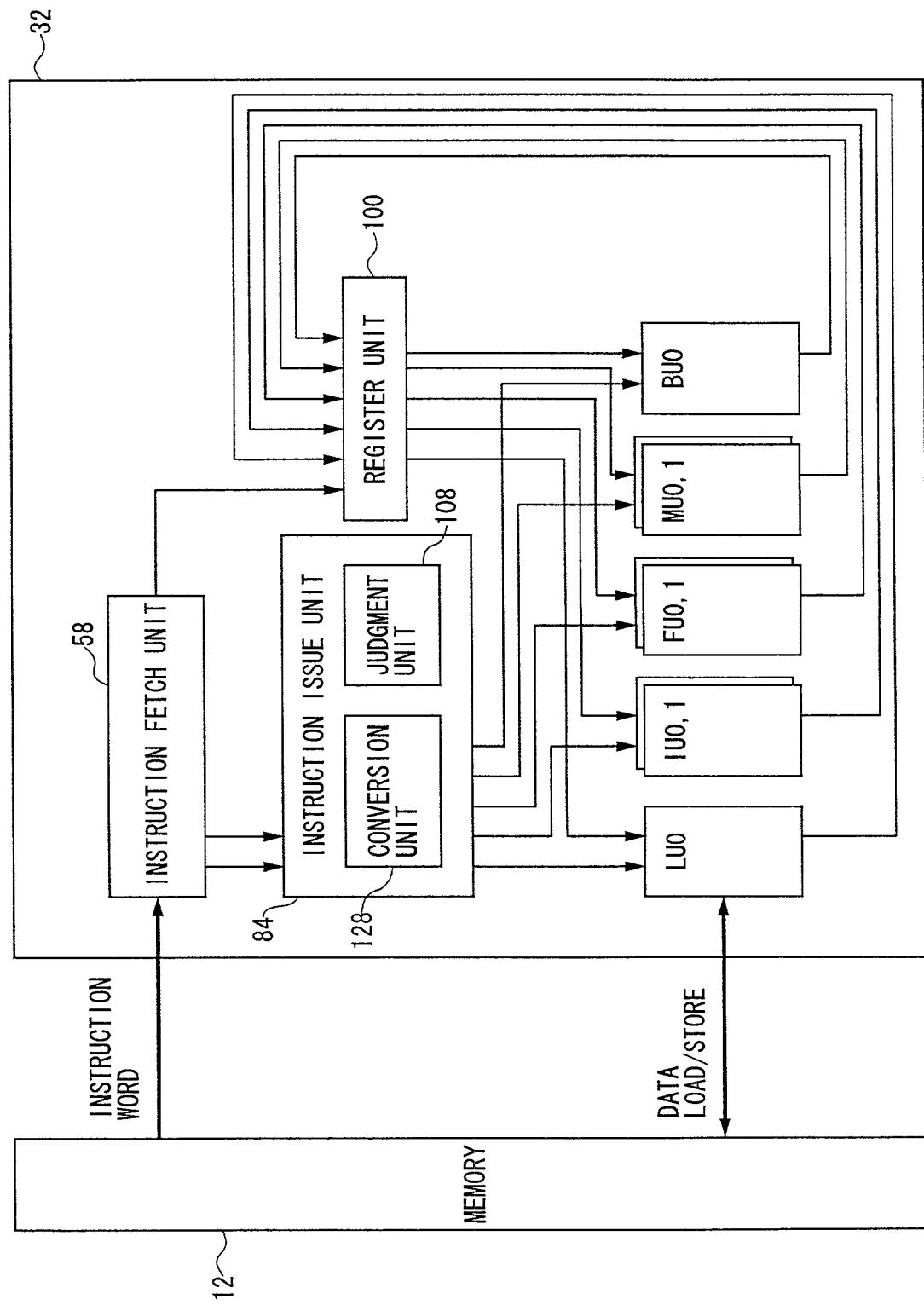


FIG.27

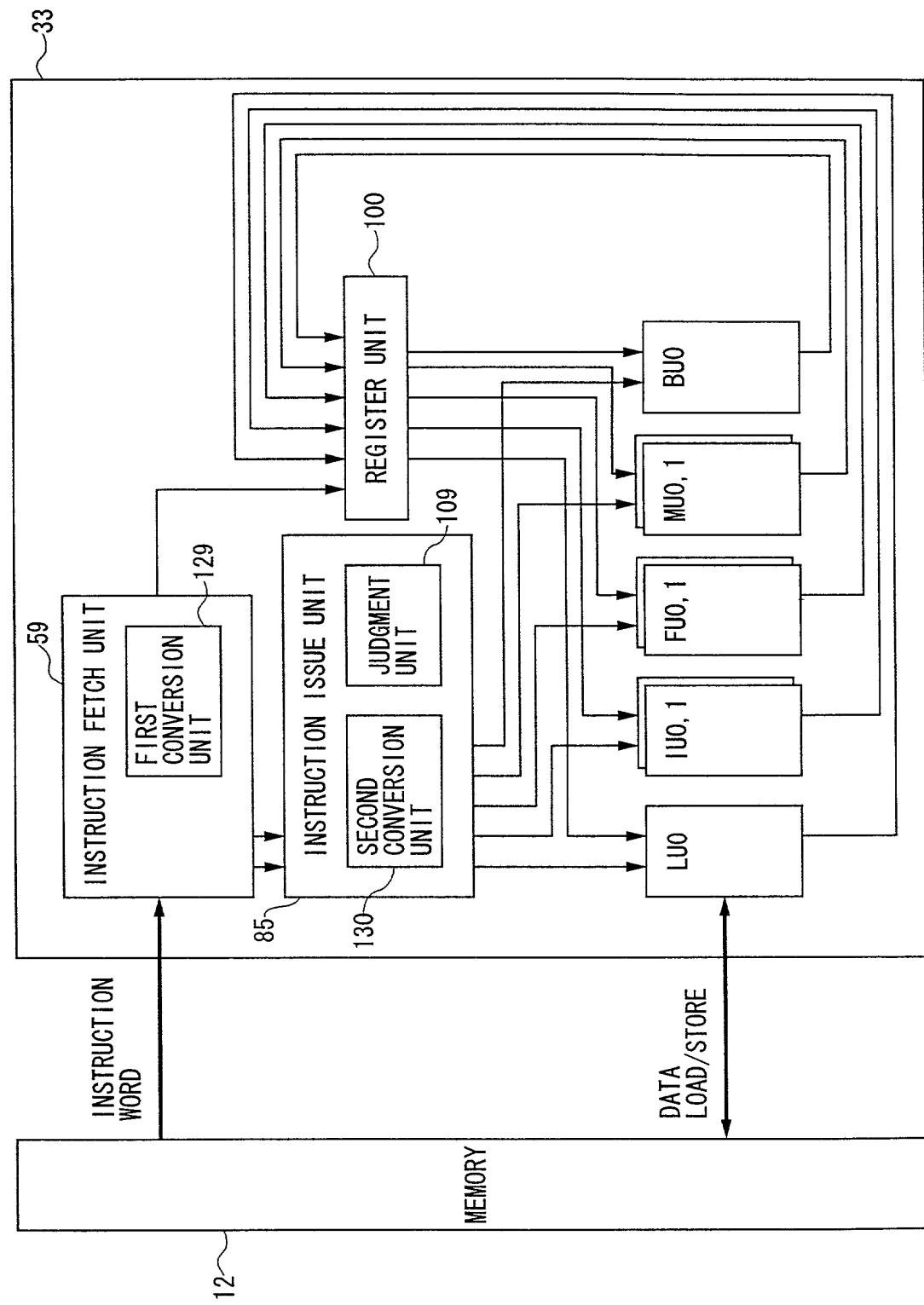


FIG. 28

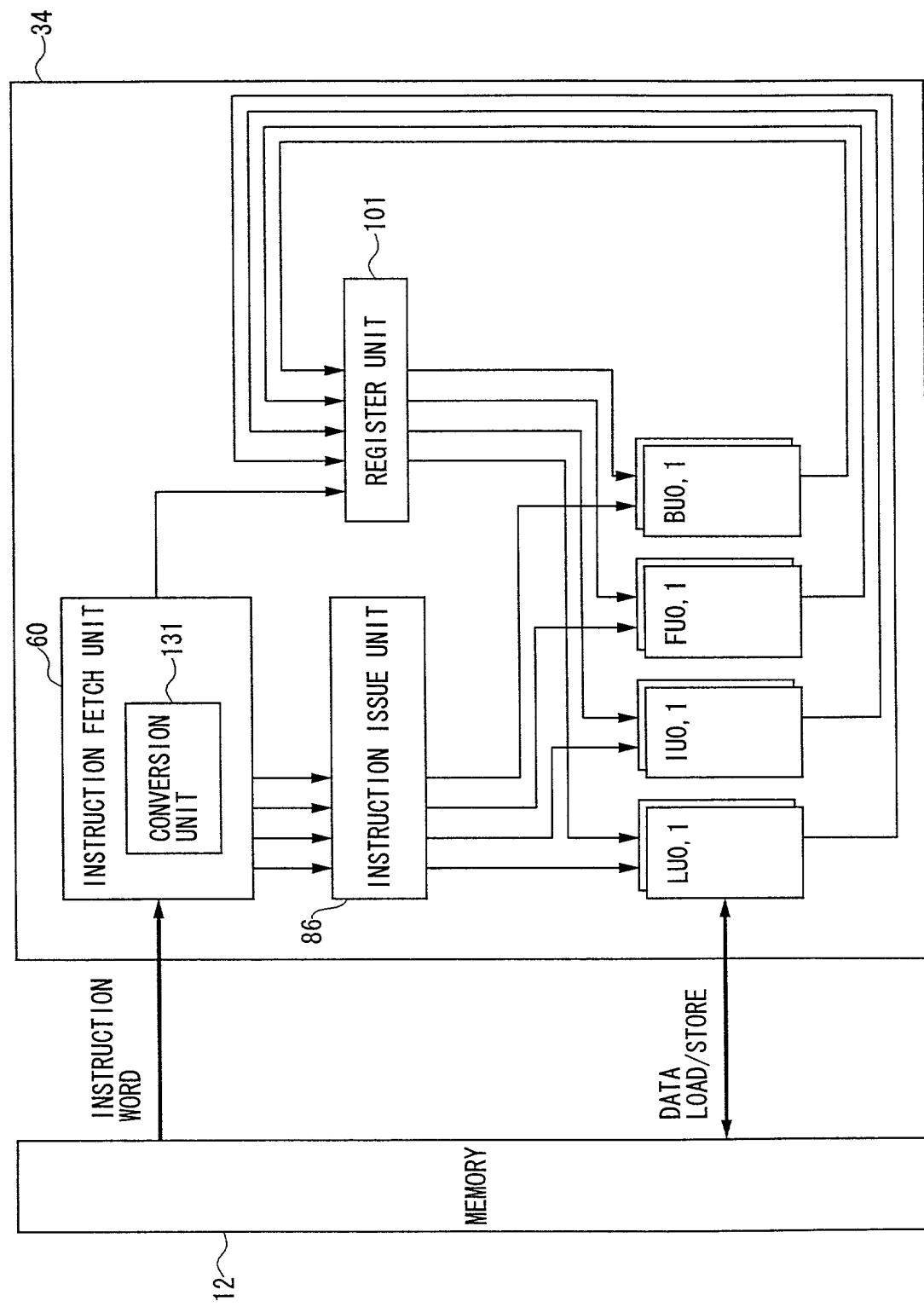


FIG.29

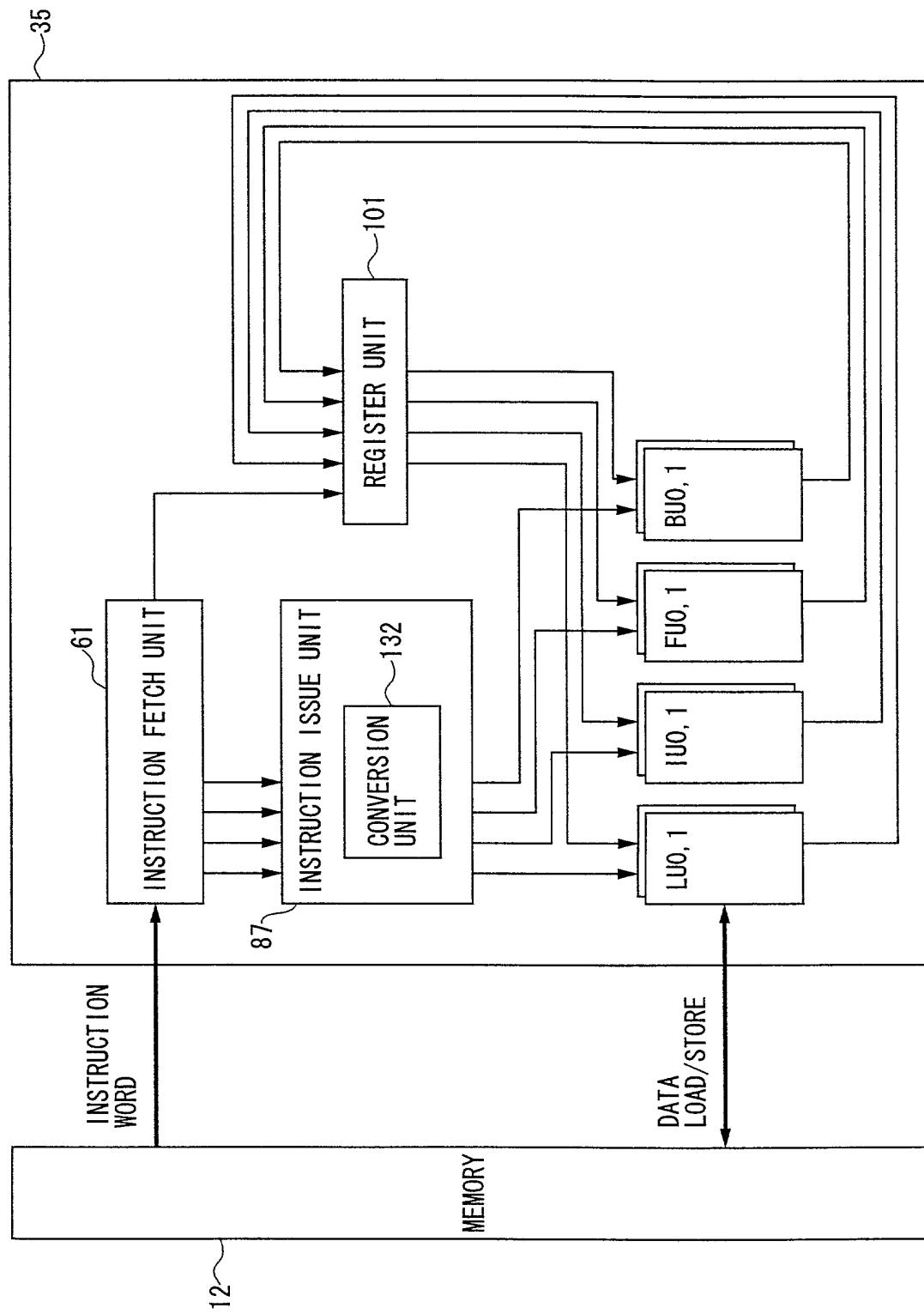


FIG.30

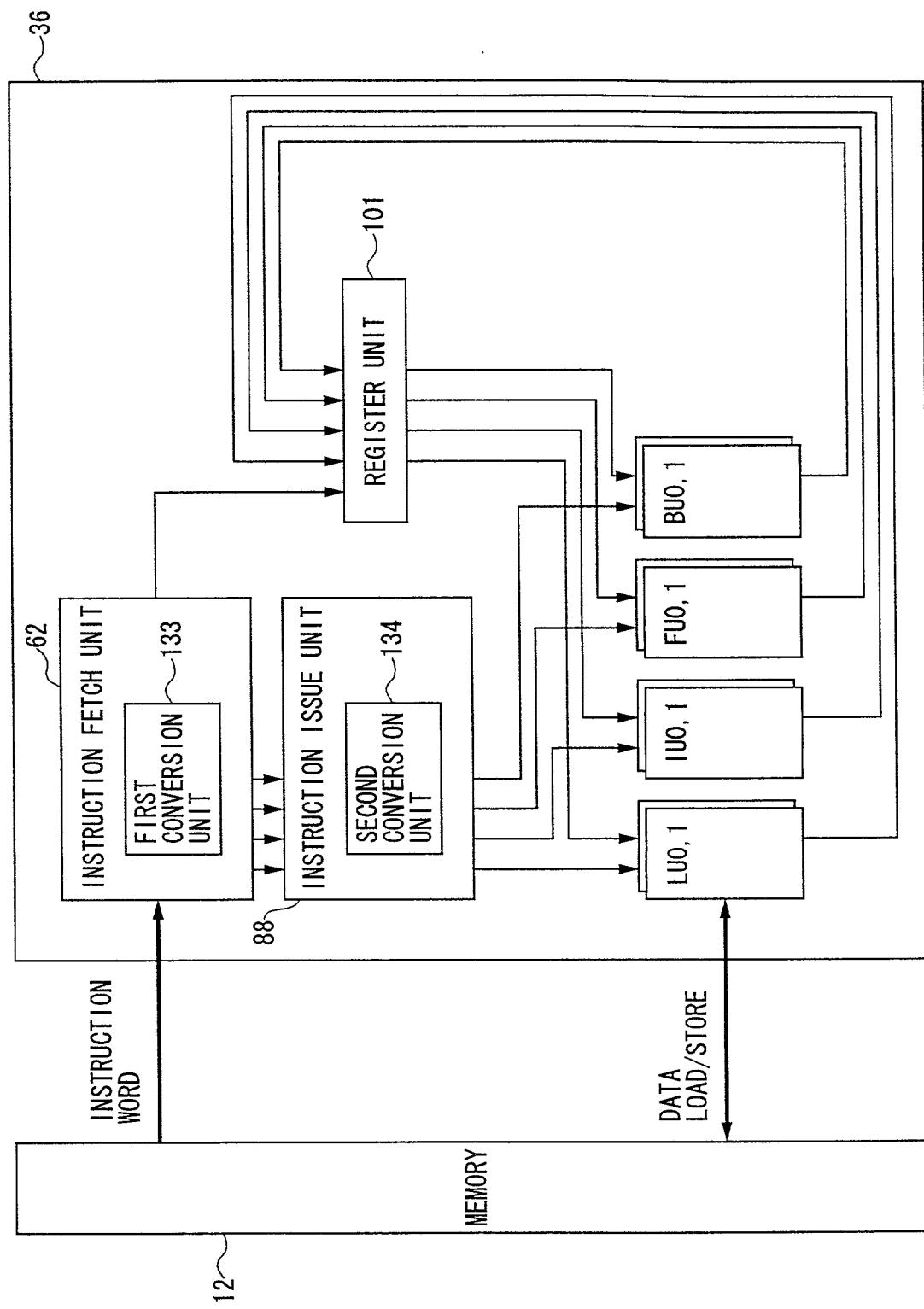


FIG. 31

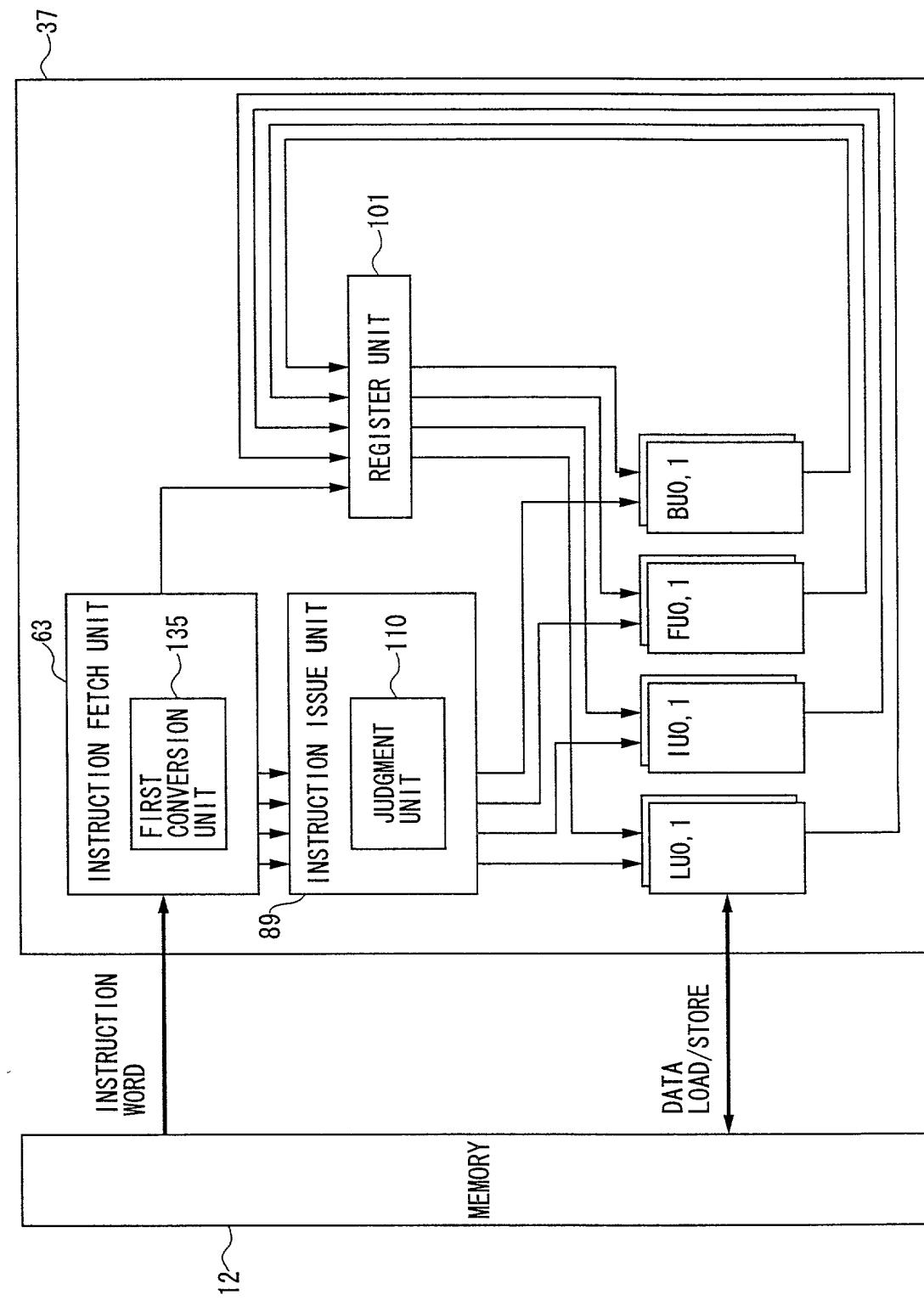


FIG. 32

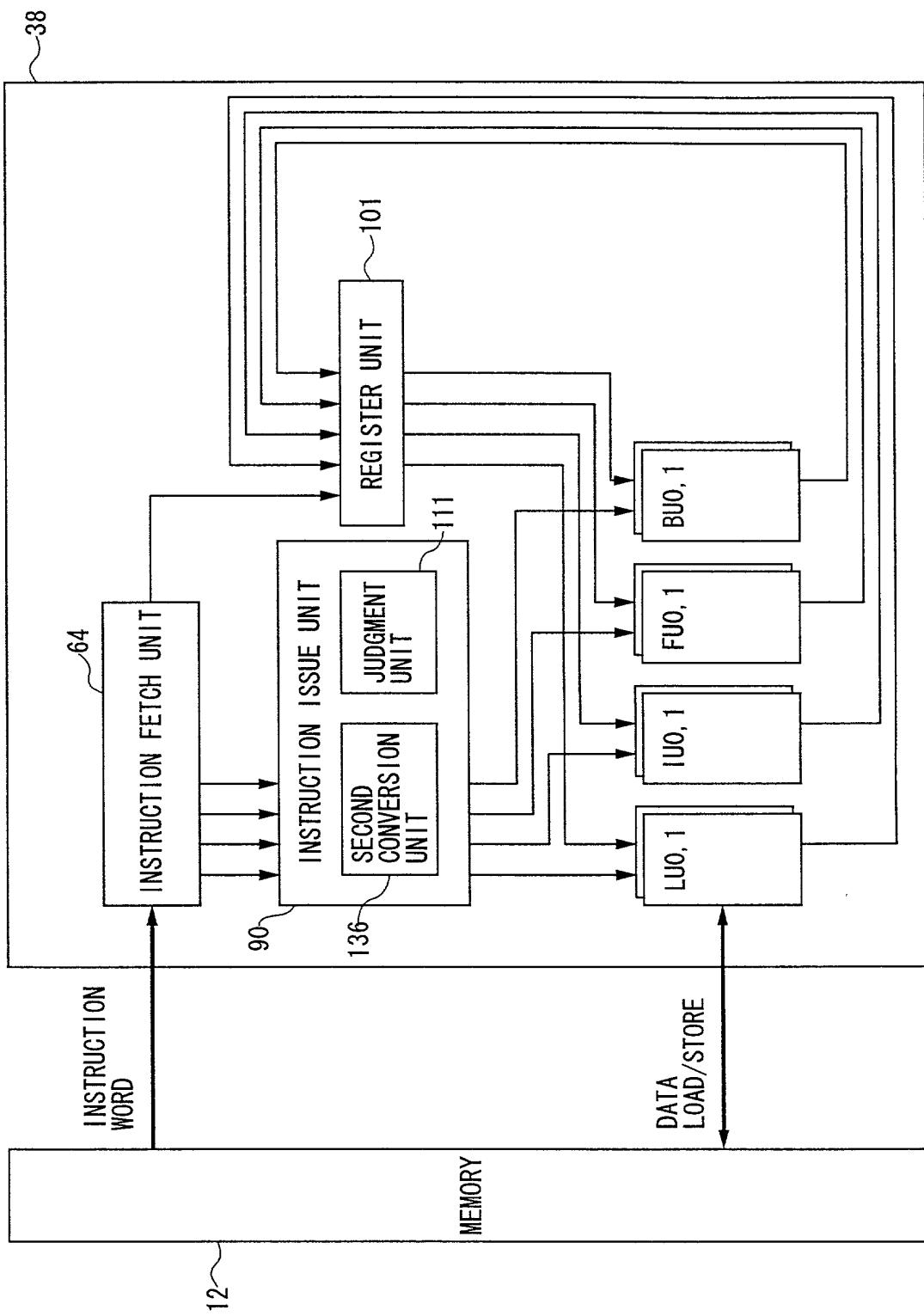


FIG.33

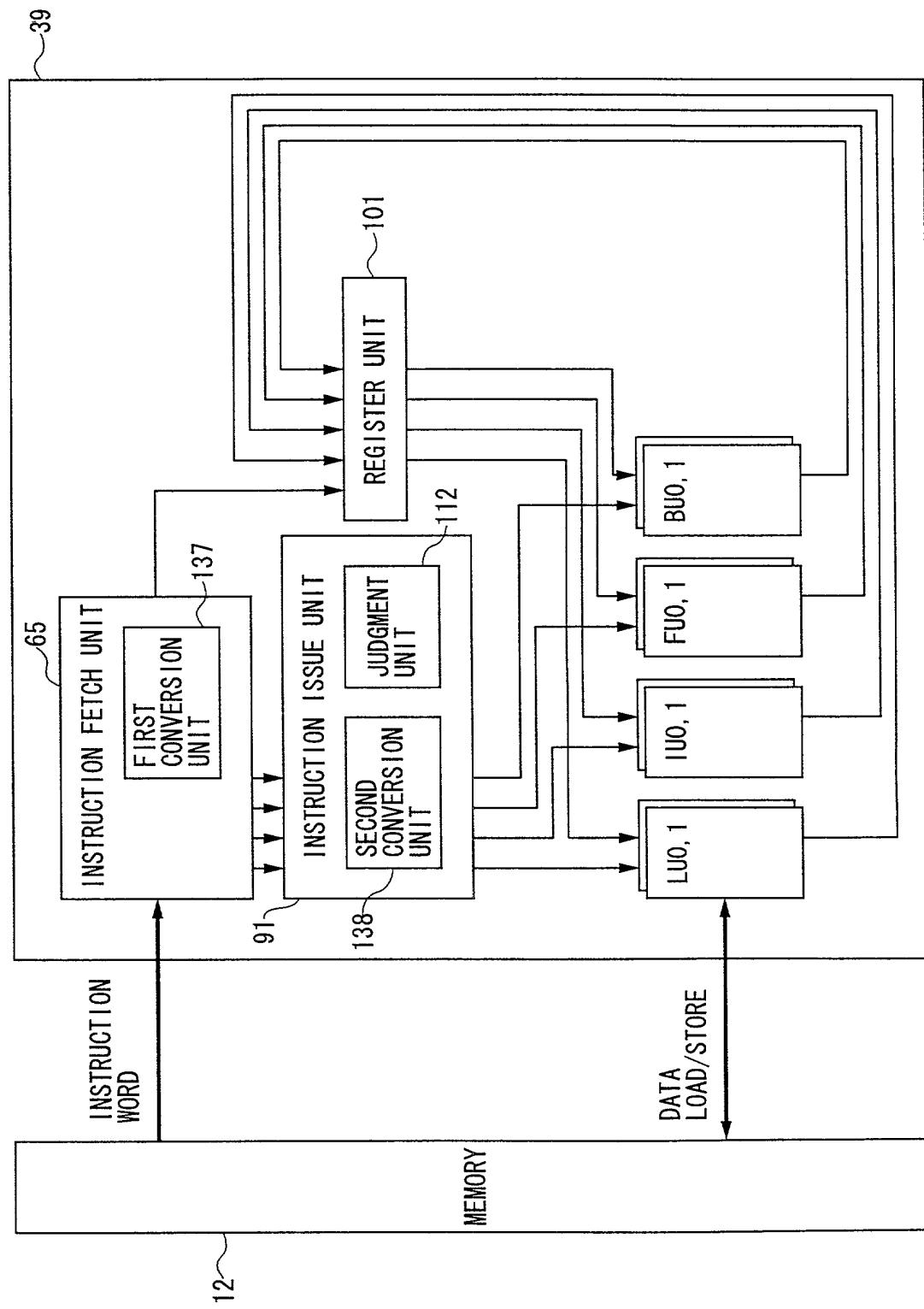


FIG. 34

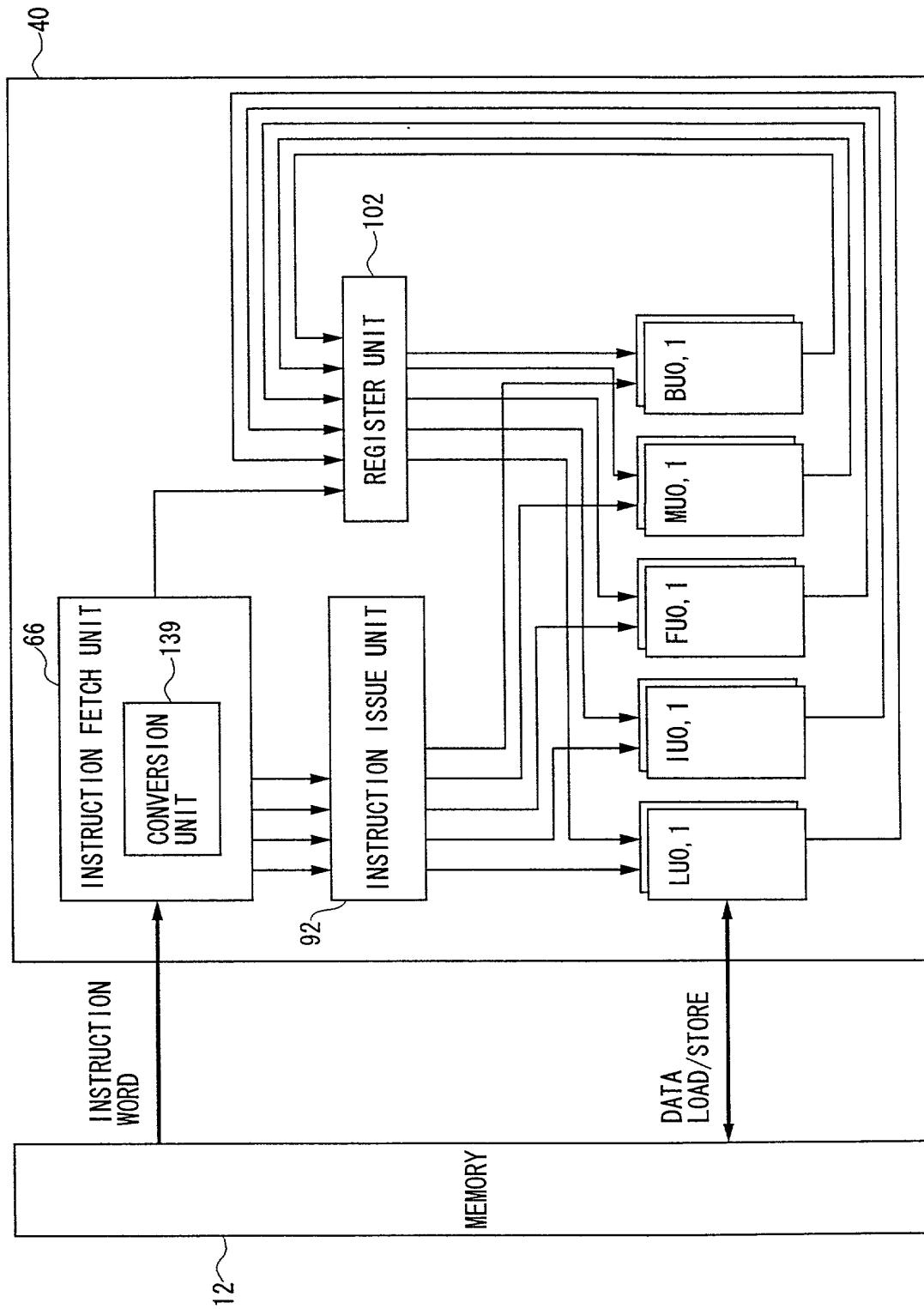


FIG. 35

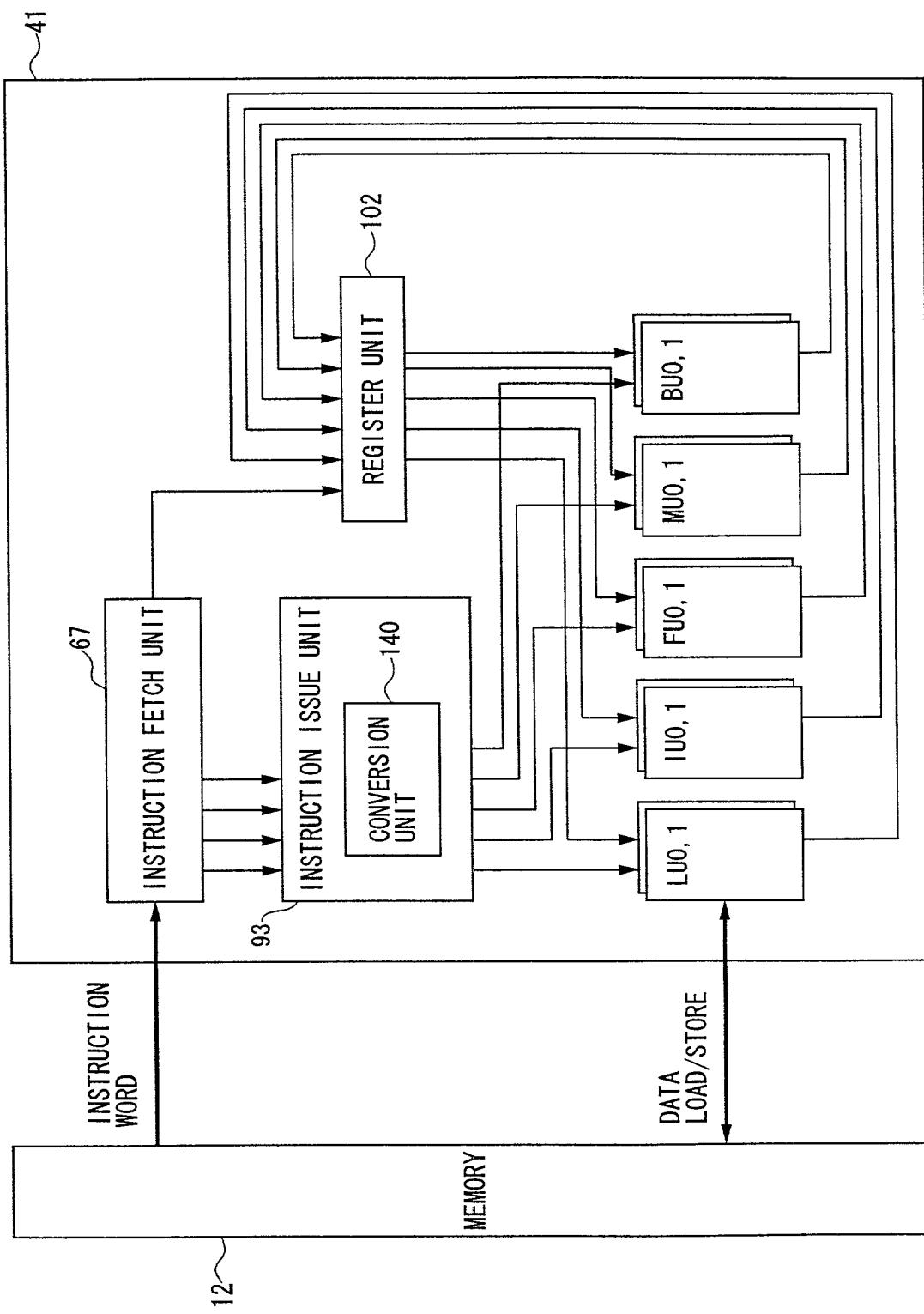


FIG.36

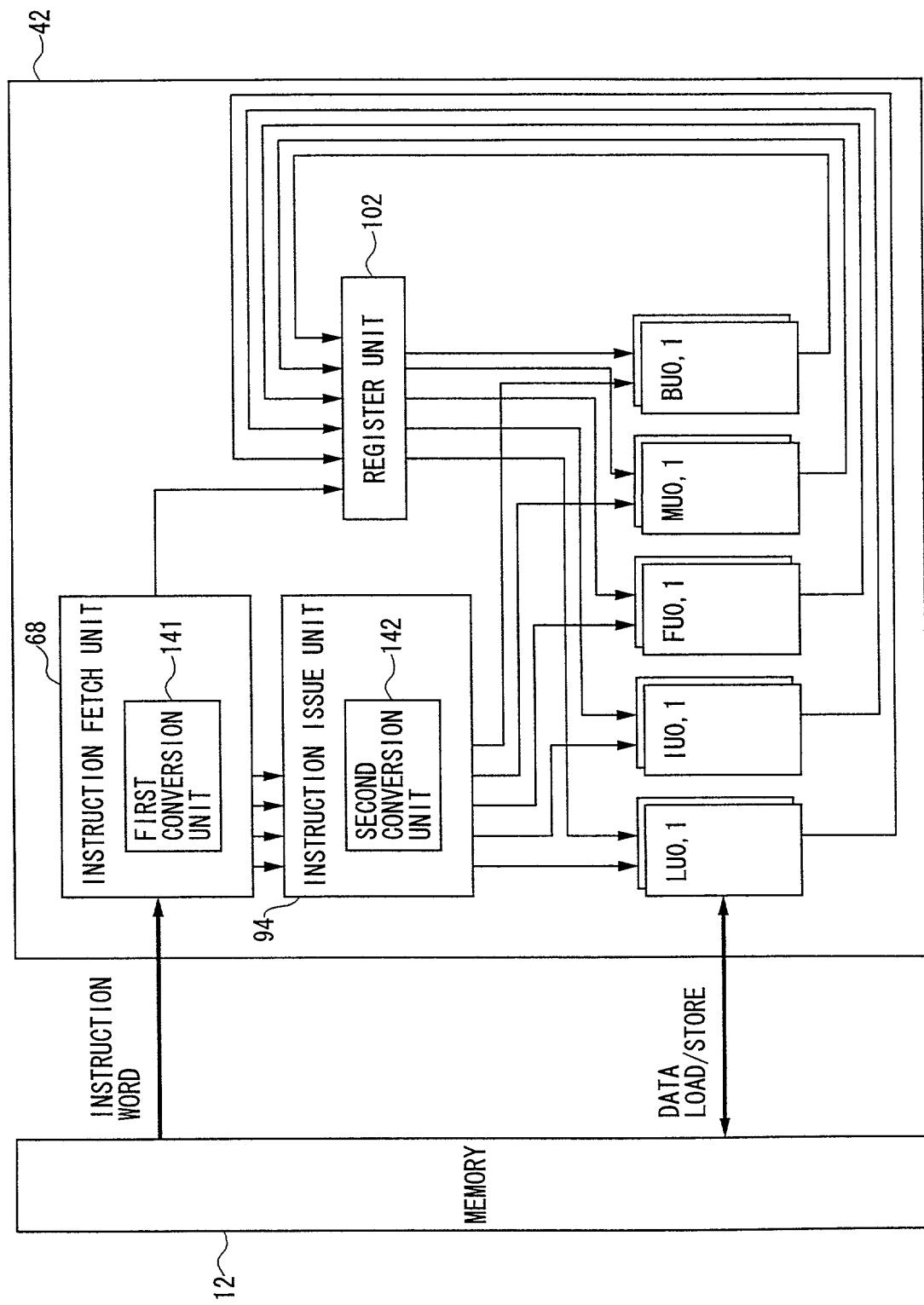


FIG. 37

43

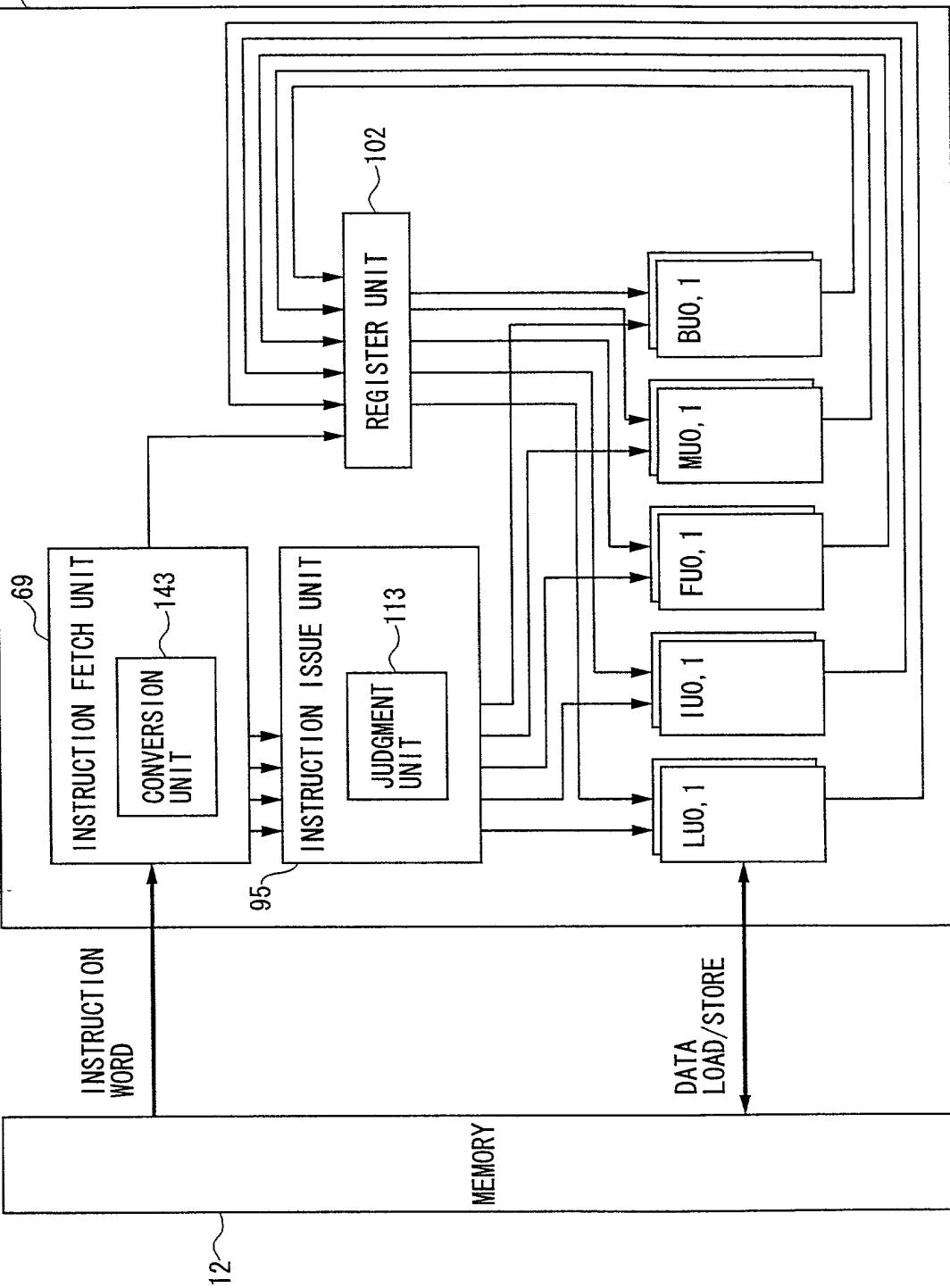


FIG. 38

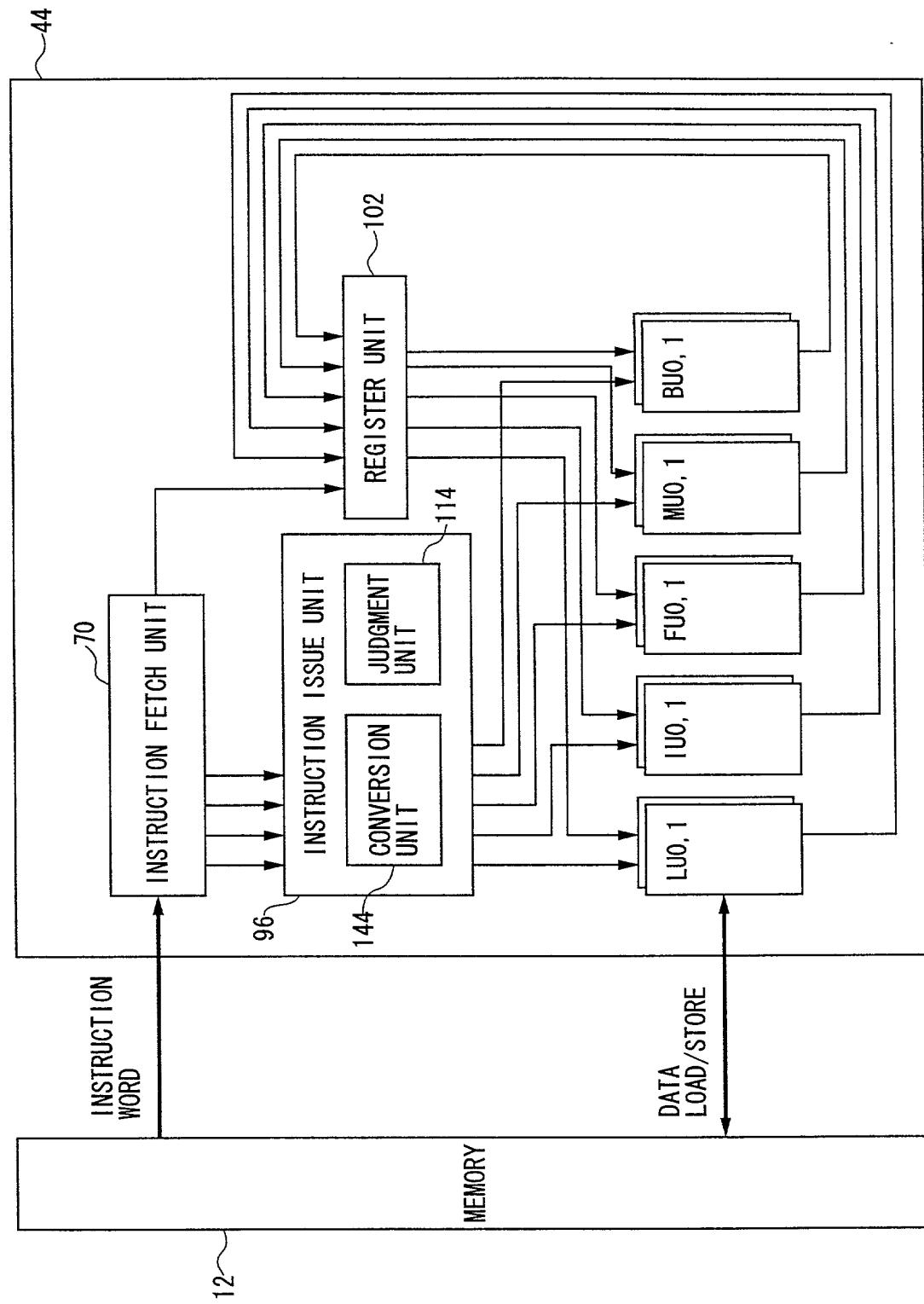
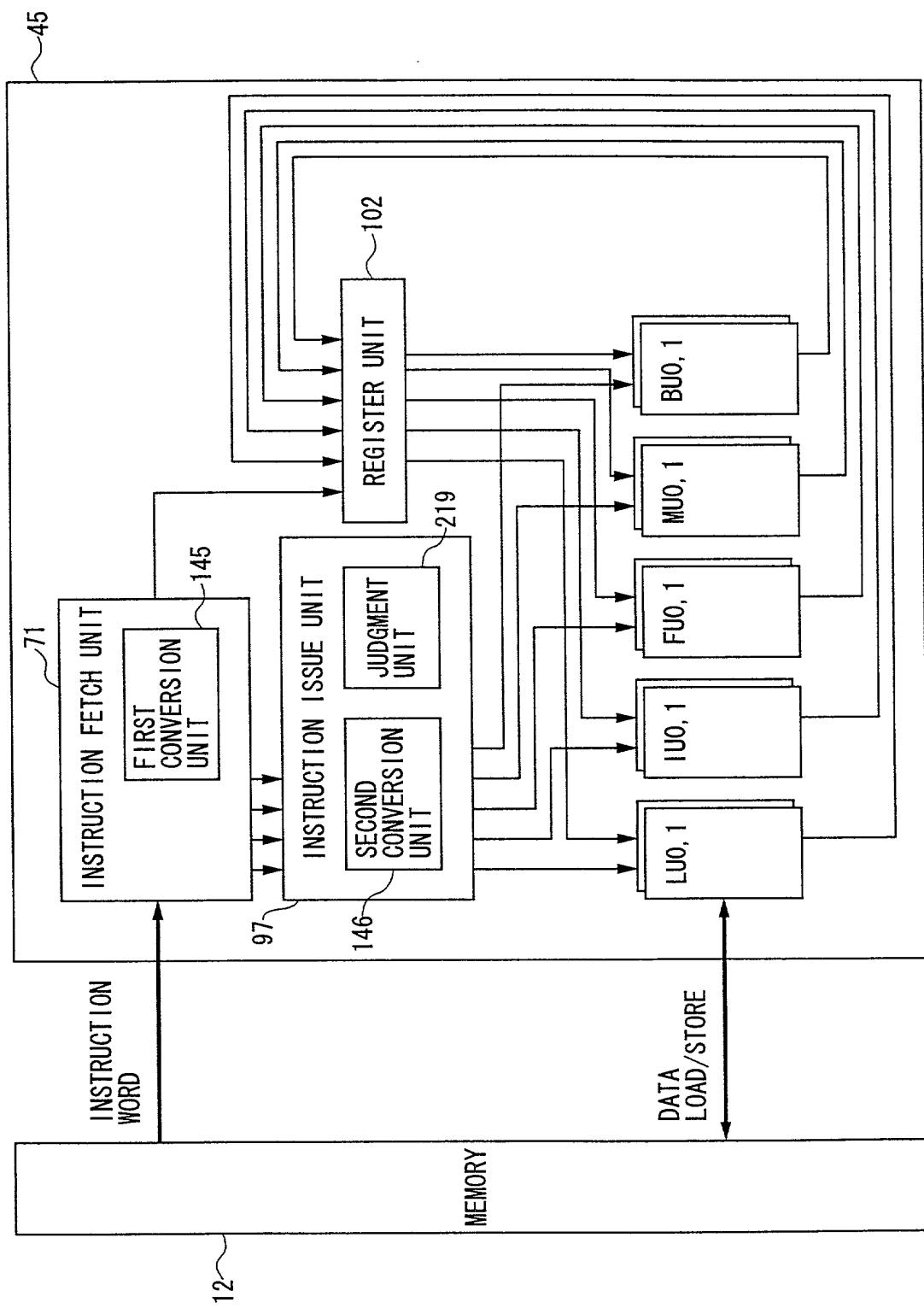


FIG.39



Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

PARALLEL PROCESSOR

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

一月一日に提出され、米国出願番号または特許協定条約国際出願番号を _____ とし、
 (該当する場合) _____ に訂正されました。

was filed on _____
 as United States Application Number or
 PCT International Application Number
 _____ and was amended on
 _____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるおり、特許資格の有無について重要な情報を開示する義務があることを認めます

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Japanese Language Declaration (日本語宣言書)

私は、米国法典第35編119条(a)-(d)又は365条(b)項に基づき下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約365条(a)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、件内をマークすることで、示しています。

Prior Foreign Application(s)

外国での先行出願

<u>Pat. Appln. No.11-281957</u>	<u>Japan</u>
(Number) (番号)	(Country) (国名)
_____	_____
(Number) (番号)	(Country) (国名)

私は、第35編米国法典119条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

<u>(Application No.)</u>	<u>(Filing Date)</u>
(出願番号)	(出願日)

私は、下記の米国法典第35編120条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条(c)に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願提出日以降で本出願の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

<u>(Application No.)</u>	<u>(Filing Date)</u>
(出願番号)	(出願日)

私は、私自身の知識に基いて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同様の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Priority Not Claimed

優先権主張なし

1/October/1999(Day/Month/Year Filed)
(出願年月日)(Day/Month/Year Filed)
(出願年月日)

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

<u>(Application No.)</u>	<u>(Filing Date)</u>
(出願番号)	(出願日)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

<u>(Status: Patented, Pending, Abandoned)</u>
(現況: 特許許可済、係属中、放棄済)

<u>(Status: Patented, Pending, Abandoned)</u>
(現況: 特許許可済、係属中、放棄済)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration

(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続を米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number)

James D. Halsey, Jr., 22,729; Harry John Staas, 22,010; David M. Pitcher, 25,908; John C. Garvey, 28,607; J. Randall Beckers, 30,358; William F. Herbert, 31,024; Richard A. Gollhofer, 31,106; Mark J. Henry, 36,162; Gene M. Garner II, 34,172; Michael D. Stein, 37,240; Paul I. Kravetz, 35,230; Gerald P. Joyce, III, 37,648; Todd E. Marlette, 35,269; Harlan B. Williams, Jr., 34,756; George N. Stevens, 36,938; Michael C. Soldner, P-41,455 and William M. Schertler, 35,348 (agent)

書類送付先

Send Correspondence to:

STAAS & HALSEY
700 Eleventh Street, N.W.
Suite 500
Washington, D.C. 20001

直接電話連絡先：（名前及び電話番号）

Direct Telephone Calls to: (name and telephone number)

STAAS & HALSEY
(202) 434-1500

唯一または第一発明者名	Full name of sole or first inventor Hideo Miyake	
発明者の署名	日付	Inventor's signature Hideo Miyake
住所	Residence Kawasaki, Japan	
国籍	Citizenship Japan	
私書箱	Post Office Address c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211-8588 Japan	
第二共同発明者	Full name of second joint inventor, if any Atsuhiko Suga	
第二共同発明者	日付	Second inventor's signature Atsuhiko Suga
住所	Residence Kawasaki, Japan	
国籍	Citizenship Japan	
私書箱	Post Office Address c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211-8588 Japan	

（第三以降の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for third and subsequent joint inventors.)

第三共同発明者	Full name of third joint inventor, if any Yasuki Nakamura		
第三共同発明者	日付	Third inventor's signature <i>Yasuki Nakamura</i>	Date August 18, 2000
住 所	Residence Kawasaki, Japan		
国 稽	Citizenship Japan		
私書箱	Post Office Address c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211-8588 Japan		
第四共同発明者	Full name of fourth joint inventor, if any Yoshimasa Takebe		
第四共同発明者	日付	Fourth inventor's signature <i>Yoshimasa Takebe</i>	Date August 18, 2000
住 所	Residence Kawasaki, Japan		
国 稽	Citizenship Japan		
私書箱	Post Office Address c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211-8588 Japan		
第五共同発明者	Full name of fifth joint inventor, if any		
第五共同発明者	日付	Fifth inventor's signature	Date
住 所	Residence		
国 稽	Citizenship		
私書箱	Post Office Address		
第六共同発明者	Full name of sixth joint inventor, if any		
第六共同発明者	日付	Sixth inventor's signature	Date
住 所	Residence		
国 稽	Citizenship		
私書箱	Post Office Address		

(第七以降の共同発明者についても同様に
記載し、署名をすること)

(Supply similar information and signature for
seventh and subsequent joint inventors.)